Model 10269A
General Purpose
Probe Interface

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General Purpose
Probe Interface

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Table of Contents

Chapter 1: Model 10269A General Purpose Probe Interface
General....1-1
Installation....1-1
Model 1630A/D Interconnect....1-2

Appendix A: Interface Module Z80
Introduction....A-1
System Configuration....A-2
Hardware Installation....A-3
Interface Description....A-5
Operation....A-7
Format Specification....A-7
User Base....A-7
The Z80 Inverse Assembler....A-8
Error Messages....A-9

Appendix B: Interface Module 68000
Introduction....B-1
System Configuration....B-2
Hardware Installation....B-3
Interface Description....B-5
Operation....B-8
Format Specification....B-8
The 68000 Inverse Assembler....B-9
Error Messages....B-10

Appendix C: Interface Module 8085
Introduction....C-1
System Configuration....C-2
Hardware Installation....C-3
Interface Description....C-5
Operation....C-7
Format Specification....C-7
User Base....C-8
The 8085 Inverse Assembler....C-8
Error Messages....C-10

Appendix D: Interface Module Z8001/Z8002
Introduction....D-1
System Configuration....D-2
Hardware Installation....D-3
Interface Description....D-5
Operation....D-10
Z8001 Format Specification....D-10
Z8002 Format Specification....D-11
The Z8001/Z8002 Inverse Assembler....D-12
Error Messages....D-13

Table of Contents (Cont'd)

Appendix E: Interface Module 8086/8088
Introduction....E-1
System Configuration....E-2
Hardware Installation....E-3
Interface Description....E-5
Operation....E-11
8086/8088 Selection....E-11
Min/Max Mode....E-11
Bus Cycle Mode (fetched instructions)....E-12
Executed Instruction Mode (dequeued)....E-12
Status Encoding....E-13
8086 Format Specification....E-15
8088 Format Specification....E-16

Appendix F: Model 10269A Options for Making a User Definable Interface
Introduction....F-1
Understanding the Target System....F-2
Bus Structure....F-3
Clock Characteristics....F-3
Status Information....F-4
DMA or Multi-Master Operation....F-4
Interrupt Structure....F-4
Operating Voltage Levels....F-4
Mechanics of Probing....F-5
Understanding the Interface Module....F-5
Clock Inputs....F-5
State Data Inputs....F-6
Signal Buffering....F-6
Setup and Hold Times....F-7
Using the 1630A/D to Demultiplex....F-7
Building the Interface Module....F-9
Components....F-9
Wave Soldering the PC Board....F-9
Components Supplied with the Wire Wrapping Interface Module....F-9
Printed Circuit Card....F-10
Wiring Pins....F-10
Connectors....F-10
Hardware....F-11
Components Supplied with the Microprocessor Interface Kit....F-12
Component Sockets....F-12
Wiring Pins....F-13
Bypass Capacitors....F-14
Power Fuse....F-14
User Supplied Components....F-15

Table of Contents (Cont'd)

Power Suppy Distribution.....F-15
  Using +5V from the 1630A/D.....F-15
  User Supplied Power.....F-15
  Bypass Capacitors.....F-16
  Power Ground Connections.....F-16
  Signal Ground Connections.....F-17
Wiring the Interface Module.....F-17
  To Target System Connectors.....F-17
  Between Components on the Interface Module.....F-18
  To General Purpose Probe Interface Connectors.....F-18
Final Assembly.....F-20
  Hardware.....F-20
  Spacers and Sheet Metal.....F-20
  Target System Cables aand Strain Relief Bracket.....F-21
Initial Power Up.....F-23
  Checking Signal and Power Wiring Connections.....F-23
  Connection to the Target System and Preprocessor.....F-23
  Verifying Operation of the Interface Module.....F-23
Optional Probe Cables for Dip Packages.....F-24
Customizing the Cable for a Particular Device.....F-26
Connecting Cable to the Interface.....F-26
Model 10269A Option Parts List and Wiring Diagram.....F-30
  Option 100--Wire Wrapping Interface Module.....F-30
  Option 101--Microprocessor Interface Kit.....F-31
  Option 102--40 Pin Cable Assembly.....F-31
  Option 103--48 Pin Cable Assembly.....F-32
  Option 104--64 Pin Cable Assembly.....F-32
Interfacing to the PDP-11 Unibus (10275A),
 LSI-11 Q-Bus (10276A), and
 Intel Multibus (52126A).....F-35
PDP-11 Unibus Interface (10275A).....F-35
LSI-11 Q-Bus Interface (10267A).....F-36
Intel Multibus Interface (52126A).....F-37

Table of Contents (Cont'd)

Appendix G: Interface Module 6800/6802
Introduction....G-1
System Configuration....G-2
Hardware Installation....G-2
Interface Description....G-5
Operation....G-8
6800/6802 Selection....G-8
Status Encoding....G-8
Format Specification....G-9
Trace Specification....G-10
The 6800/6802 Inverse Assembler....G-10
Error Messages....G11

Appendix H: Interface Module NSC800
Introduction....H-1
System Configuration....H-2
Hardware Installation....H-2
Interface Description....H-5
Operation....H-7
Format Specification....H-7
The NSC800 Inverse Assembler....H-8
Error Messages....H-8

List of Illustrations

Figure A-1. ZIF Socket Assembly, Exploded View.....A-4
Figure A-2. Z80 Interface Block Diagram.....A-5
Figure A-3. Z80 Format Specification.....A-7
Figure A-4. Z80 Status Map.....A-8
Figure B-1. ZIF Socket Assembly, Exploded View.....B-4
Figure B-2. 68000 Interface Block Diagram.....B-5
Figure B-3. 68000 Format Specification.....B-8
Figure C-1. ZIF Socket Assembly, Exploded View.....C-4
Figure C-2. 8085 Interface Block Diagram.....C-5
Figure C-3. 8085 Format Specification.....C-7
Figure C-4. 8085 Status Map.....C-8
Figure D-1. ZIF Socket Assembly, Exploded View.....D-4
Figure D-2. Z8001/Z8002 Interface Block Diagram.....D-6
Figure D-3. Z8001 Format Specification.....D-10
Figure D-4. Z8002 Format Specification.....D-11
Figure E-1. ZIF Socket Assembly, Exploded View.....E-4
Figure E-2. 8086/8088 Interface Block Diagram.....E-7
Figure E-3. 8086 Format Specification.....E-15
Figure E-4. 8088 Format Specification.....E-16
Figure F-1. Wire Wrapping Interface Module
Component Loading Diagram.....F-11
Figure F-2. Microprocessor Interface
Kit Component Loading Diagram.....F-13
Figure F-3. Power Distribution Wiring Diagram.....F-16
Figure F-4. Wire Wrapping Module Exploded View.....F-21
Figure F-5. Target Cable Installation.....F-22
Figure F-6. Probe Cable Assembly Exploded View.....F-25
Figure F-7. Diagram of 40-Pin Probe Cable.....F-26
Figure F-8. Diagram of 48-Pin Probe Cable.....F-27
Figure F-9. Diagram of 64-Pin Probe Cable.....F-28
Figure F-10. Wire Wrapping Interface Module Wiring
Diagram.....F-33
Figure F-11. PDP-11 Format Specification.....F-36
Figure F-12. LSI-11 Format Specification.....F-36
Figure F-13. Intel Multibus Format Specification.....F-37
Figure F-14. Wire Wrap Board Wiring For 10275A.....F-39
Figure F-15. Wire Wrap Board Wiring For 10276A.....F-41
Figure F-16. Wire Wrap Board Wiring For 52126A.....F-43
Figure G-1. Interface Cable Assembly, Exploded View.....G-4
Figure G-2. Block Diagram of the 6800/6802 Interface.....G-5
Figure G-3. Block Diagram of the State Machine for
Decoding the 6800/6802 Status.....G-6
Figure G-4. 6800/6802 Format Specification.....G-9
Figure G-5. 6800/6802 Status Map.....G-9
Figure G-6. 6800/6802 Trace Specification.....G-10
Figure H-1. ZIF Socket Assembly, Exploded View.....H-4
Figure H-2. NSC800 Interface Block Diagram.....H-5
Figure H-3. NSC800 Format Specification.....H-7

List of Tables

Table A-1. Interface Module Specifications.....A-1
Table A-2. Z80 Signal List.....A-6
Table B-1. Interface Module Specifications.....B-1
Table B-2. 68000 Signal List.....B-6
Table C-1. Interface Module Specifications.....C-1
Table C-2. 8085 Signal List.....C-6
Table D-1. Interface Module Specifications.....D-1
Table D-2. Z8001 Signal List.....D-6
Table D-3. Z8002 Signal List.....D-8
Table E-1. Interface Module Specifications.....D-1
Table E-2. 8086 Signal List.....E-8
Table E-3. 8088 Signal List.....E-10
Table E-4. STATUS Field Encoding.....E-14
Table F-1. Interface Module Specifications.....F-2
Table F-2. Wire Wrapping Interface Module Components F-10
Table F-3. Microprocessor Interface Kit Components F-12
Table F-4. Interface Signal Interconnections.....F-18
Table F-5. Hardware Provided F-20
Table F-6. 40-Pin Probe Cable Interconnections.....F-27
Table F-7. 48-Pin Probe Cable Interconnections.....F-28
Table F-8. 64-Pin Probe Cable Interconnections.....F-29
Table F-9. Option 100--Wire Wrapping
Interface Module Parts List.....F-30
Table F-10. Option 101--Microprocessor
Interface Kit Parts List.....F-31
Table F-11. Option 102, 40-Pin Cable Assembly Parts List.....F-31
Table F-12. Option 103, 48-Pin Cable Assembly Parts List.....F-32
Table F-13. Option 104, 64-Pin Cable Assembly Parts List.....F-32
Table F-14. Manufacturers' Code List.....F-32
Table F-15. Connections For 1630D to PDP-11 Via
Interface 10275A.....F-38
Table F-16. Connections For 1630D to LSI-11 Via
Interface 10276A.....F-40
Table F-17. Connections for 1630D to Intel Multibus
Via Interface 52126A.....F-42
Table F-18. Status Line Mnemonics Definitions.....F-44
Table G-1. Interface Module Specifications.....G-1
Table G-2. 6800/6802 Signal List.....G-7
Table H-1. Interface Module Specifications.....H-1
Table H-2. NSC-800 Signal List.....H-6

Chapter 1

Model 10269A

General Purpose Probe Interface

General

The HP 10269A General Purpose Probe Interface is a versatile probe. With an interface module installed, it provides a flexible and convenient probe for the HP 1630A/D Logic Analyzer. The mini-cassette supplied with the interface module contains the appropriate setups for the [Assignment] menu, and the [User Base] menu (where applicable) of the Format Specification, and an inverse assembler routine that allows the logic analyzer to display microprocessor data in the assembly language of the corresponding microprocessor.

Processor-specific interface modules with corresponding mini-cassettes are available for many of the most popular microprocessors. By using the appropriate processor-specific interface module and mini-cassette, you can quickly probe the 8-bit or 16-bit microprocessor target system or target system bus of your choice.

The processor-specific interface modules contain buffers and gating circuits. The buffers supply address, data, clock, and status signals from the target system to the pod connectors on the general purpose probe interface. For detailed descriptions of specific interface modules, refer to the appropriate appendices in this manual.

A user-definable interface module is also available. It can be configured through a wire-wrap interface to specific test ports in your system, or tailored to a specific hookup for a custom processor. Refer to appendix F in this manual.

Installation

The interface module is installed in the underside of the general purpose probe interface. It is connected to the general purpose probe interface by two internal cables.

Model 1630A/D Interconnect

Connect the probe pods from the Model 1630A/D Logic Analyzer into the pod sockets (labeled A through E) on the general purpose probe interface. The arrangement of the pods depends upon which interface module is installed. Refer to the appropriate appendix in this manual for specific connection instructions.

Connect the general purpose probe interface to the target system using the ribbon cable from the interface module. Refer to the appropriate appendix in this manual for specific instructions.

Appendix A

Interface Module

Z80

Introduction

The Model 64683A Processor Interface Module, when installed in the Model 10269A General Purpose Probe Interface, provides a complete interface between any Z80 target system and the Model 1630A/D Logic Analyzer. The interface module connects all of the Z80 target microprocessor signals to the logic analyzer inputs, along with all of the status and clock signals required for inverse assembly of the Z80 instruction set.

The Z80 configuration software on the mini-cassette sets up the [Assignment] menu of the logic analyzer format specification for compatibility with the Z80 microprocessor, and assigns names to values found on the Z80 status bus. It also contains the inverse assembler routine required to obtain displays of Z80 data in assembly language mnemonics. The interface module specifications are given in table A-1.

Table A-1. Interface Module Specifications

Processor Compatibility:	Zilog Z80 and all microprocessors made by other manufacturers which comply with Zilog Z80 specifications.
Maximum Clock Speed:	6 MHz clock output from microprocessor.
Signal Line Loading:	One LS TTL load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.30 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.
Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for analysis of a Z80 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 083 which includes:

   (1). 64683A Interface Module for Z80 microprocessors, including an Z80 interface circuit card and cable assembly.

   (2). Z80 inverse assembler and Format Specification setups on Minicassette HP Part No. 64683-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the Z80 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure A-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure A-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

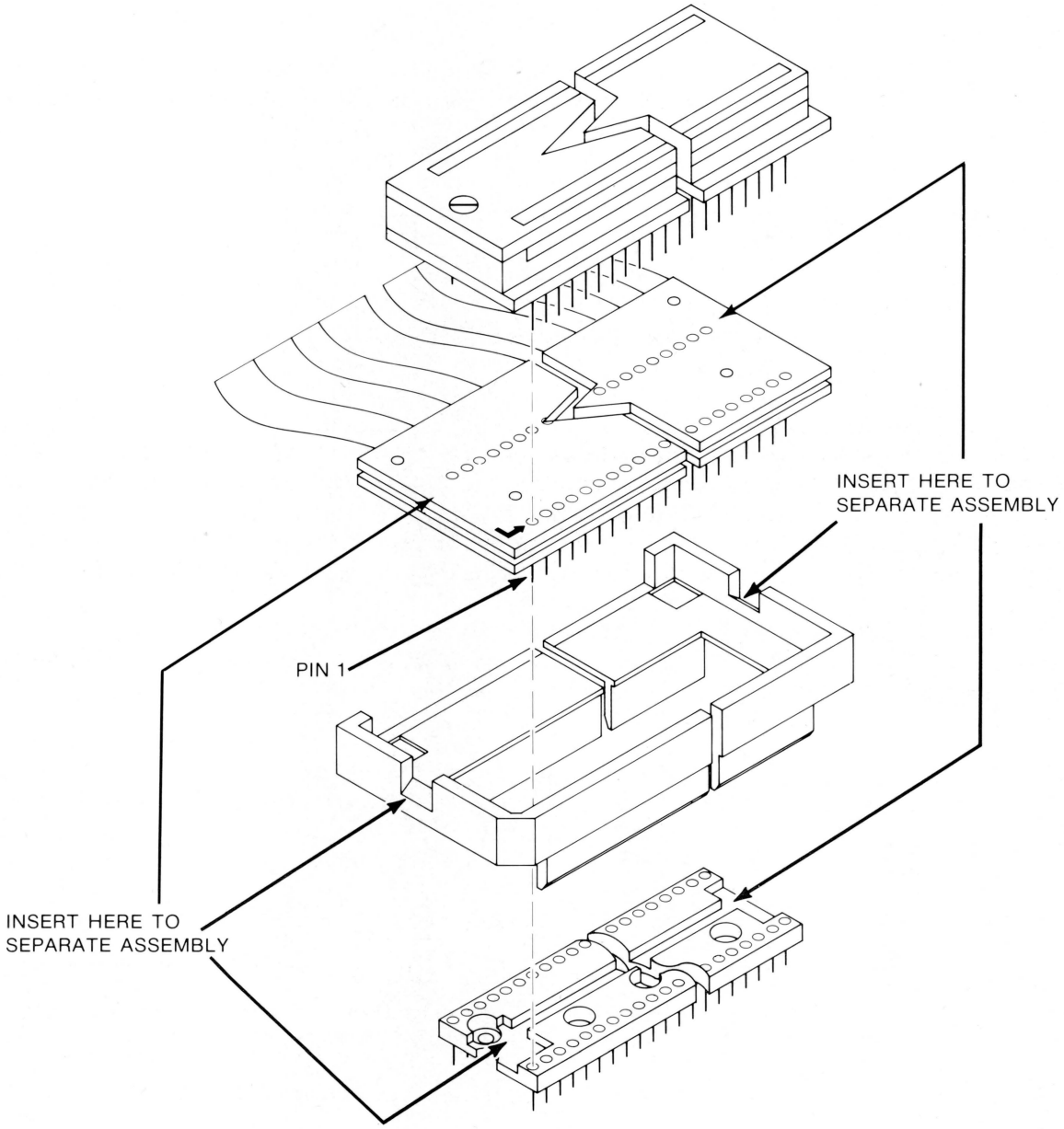

Figure A-1. ZIF Socket Assembly, Exploded View

General Purpose
Probe Interface

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	1
B	4
C	2
D	3
E	n/c

Interface Description

The Z80 microprocessor uses a nonmultiplexed bus. Address and some status signals are valid throughout the cycle. Data is valid at the end of the cycle. The remaining status is derived from WR, LIORQ, and LRFSH. The inverted LMREQ and LIORQ signal are used as OR'ed clocks to enter information into the logic analyzer (see figure A-2 for the Z80 interface block diagram). Address, data, and status lines are buffered, or buffered and inverted, as required.

Table A-2 lists the CPU signals and cable lines on which those signals are carried to the logic analyzer.

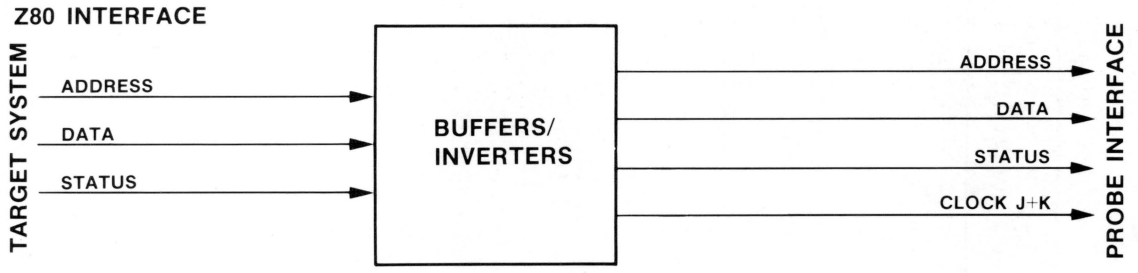

Figure A-2. Z80 Interface Block Diagram

Table A-2. Z80 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
LMREQ	19	(Clock)	4	J CLK
LIORQ	20	(Clock)	3	K CLK
A0	30	ADDRESS	2	0
A1	31	ADDRESS	2	1
A2	32	ADDRESS	2	2
A3	33	ADDRESS	2	3
A4	34	ADDRESS	2	4
A5	35	ADDRESS	2	5
A6	36	ADDRESS	2	6
A7	37	ADDRESS	2	7
A8	38	ADDRESS	2	8
A9	39	ADDRESS	3	0
A10	40	ADDRESS	3	1
A11	1	ADDRESS	3	2
A12	2	ADDRESS	3	3
A13	3	ADDRESS	3	4
A14	4	ADDRESS	3	5
A15	5	ADDRESS	3	6
D0	14	DATA	1	0
D1	15	DATA	1	1
D2	12	DATA	1	2
D3	8	DATA	1	3
D4	7	DATA	1	4
D5	9	DATA	1	5
D6	10	DATA	1	6
D7	13	DATA	1	7
WR	22	STATUS	4	0
LIORQ	20	STATUS	4	1
LRFSH	28	STATUS	4	2
LMI	27	STATUS	4	3

Operation

The logic analyzer will automatically be configured for state analysis when you load the inverse assembler from the digital cassette drive.

Format Specification

When using the Z80 interface module, the format specification will be set up by the mini-cassette software as shown in figure A-3.

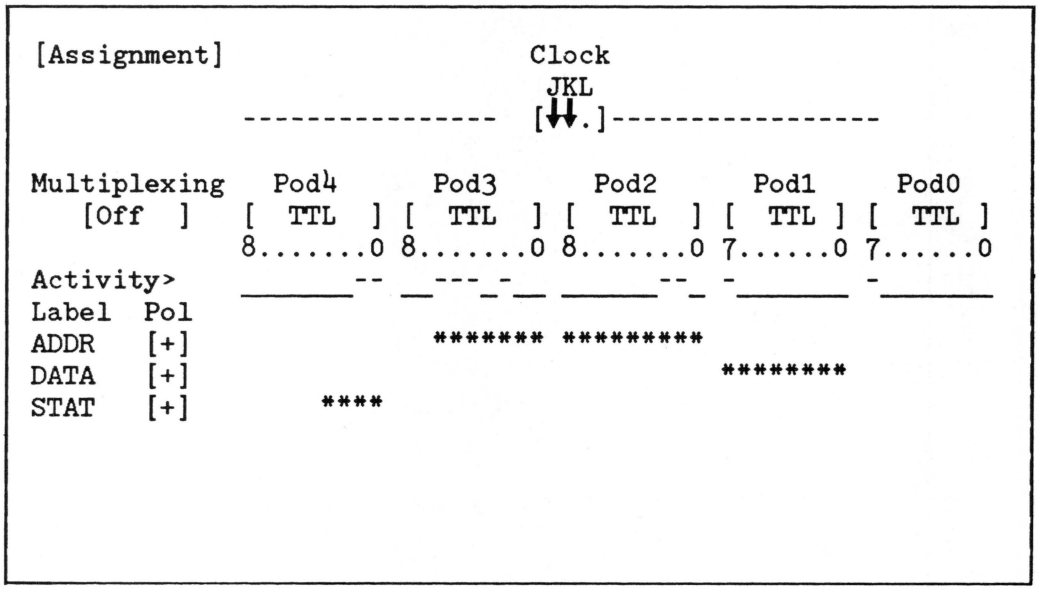

Figure A-3. Z80 Format Specification

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display of the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The LMREQ signal is input to the logic analyzer as Clock J, and LIORQ as Clock K. Both signals are inverted on the interface module, and as a result, the clock negative edge is the active edge. The LRFSH signal is input on bit 2 of Pod 4 as a qualifier to prevent the storage of refresh cycles that are not needed. A high level will inhibit refresh cycles.

User Base

The User Base menu of the format specification is set up with names to identify values found on the status label. See figure A-4.

State Format Specification

[User Base]

State Labels

Value [BIN]	STAT	
0000		
0001		
0010		
0011		
0100	intak	(interrupt acknowledge)
0101		
0110	opfch	(opcode_fetch)
0111		
1000		
1001		
1010	rfrsh	(refresh)
1011		
1100	io rd	(I/O_read)
1101	io wr	(I/O_write)
1110	memrd	(memory read)
1111	memwr	(memory write)

Figure A-4. Z80 Status Map

The Z80 Inverse Assembler

The Z80 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that one byte of an expected (single or double byte) operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that both bytes of a double-byte operand were not stored.

Examples:

JP	**57	indicates that last byte of destination address was not stored.
LD	DE,****	indicates that neither operand byte was stored.

In general, asterisks indicate that expected operand fetches are not stored in logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

Error Messages

The following list of messages will help you identify operation errors.

Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.

Illegal Opcode - undefined opcode encountered. CPU action is indeterminate.

Partial Instruction - an opcode (or opcodes) of a multi-opcode instruction was not stored in the logic analyzer.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Appendix B

Interface Module
68000

Introduction

The Model 64670A Processor Interface Module, when installed in the Model 10269A General Purpose Probe Interface, provides a complete interface between any 68000 target system and the Model 1630A/D Logic Analyzer. The interface module connects signals from the 68000 target microprocessor to the logic analyzer inputs, and generates all status and clock signals required for inverse assembly of the 68000 instruction set.

The 68000 configuration software on the mini-cassette sets up the [Assignment] menu of the logic analyzer format specification for compatibility with the 68000 microprocessor, and assigns names to values found on the 68000 status bus. It also contains the inverse assembler routine required to obtain displays of 68000 data in assembly language mnemonics. The interface module specifications are given in table B-1.

Table B-1. Interface Module Specifications

Processor Compatibility:	Motorola MC68000 and all microprocessors made by other manufacturers which comply with Motorola MC68000 specifications.
Maximum Clock Speed:	12 MHz clock input to microprocessor.
Signal Line Loading:	One LS TTL load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.4 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.
Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for logic analysis of the 68000 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 070 which includes:

   (1). 64670A Interface Module for 68000 microprocessors, including an 68000 interface circuit card and cable assembly.

   (2). 68000 inverse assembler and Format Specification setups on Minicassette HP Part No. 64670-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the 68000 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure B-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure B-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

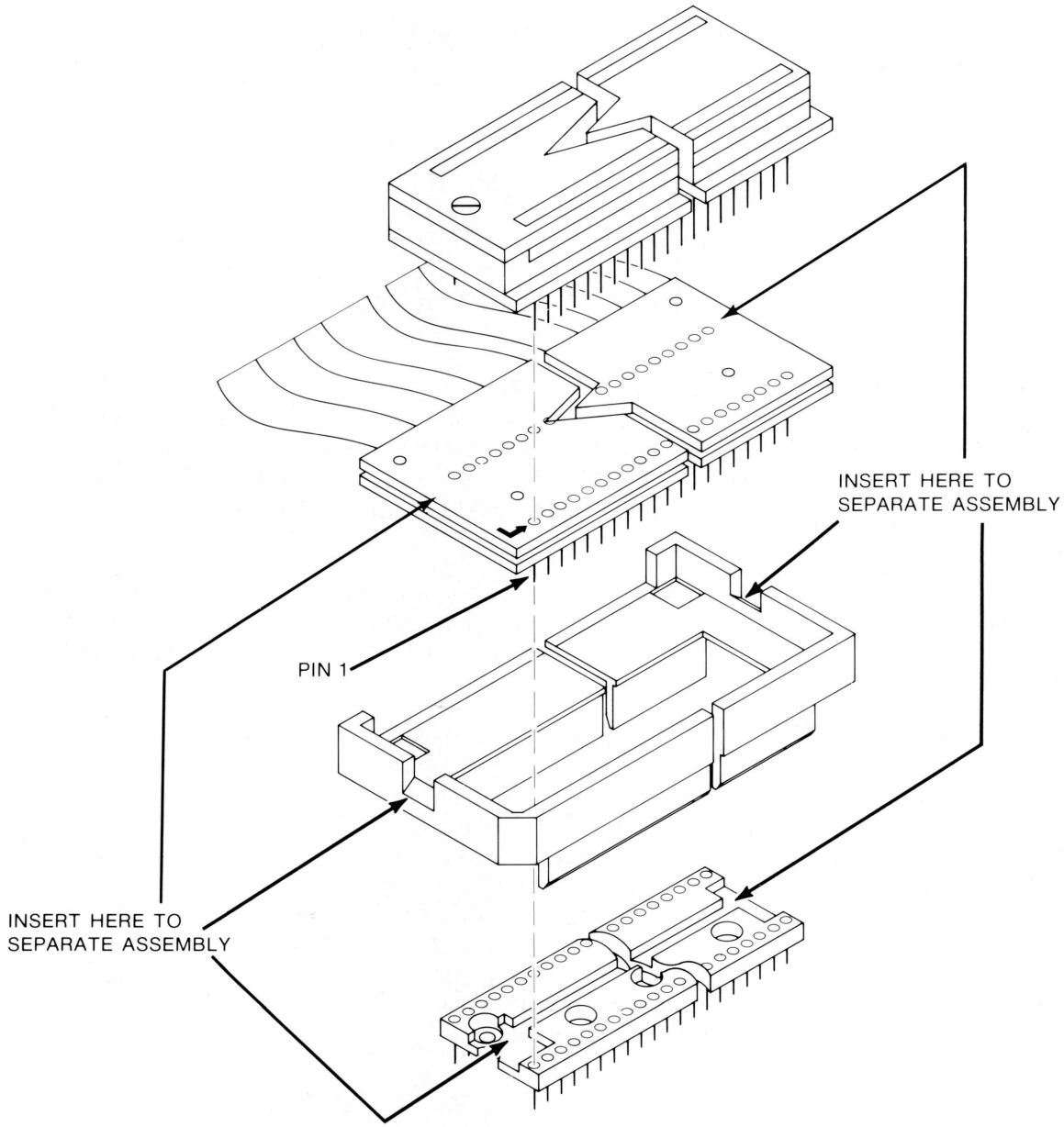

Figure B-1. ZIF Socket Assembly, Exploded View

General Purpose
Probe Interface

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	0
B	1
C	2
D	3
E	4

Interface Description

The 68000 interface circuit is comprised, primarily, of buffers. Generation of most status signals is accomplished by these devices. Figure B-2 shows the 68000 interface block diagram.

Table B-2 lists the CPU signals and cable lines on which those signals are carried to the logic analyzer.

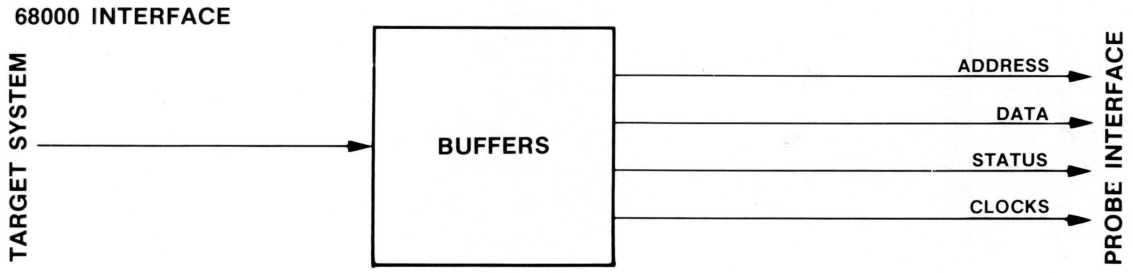

Figure B-2. 68000 Interface Block Diagram

Table B-2. 68000 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AS	6	(Clock)	4	J CLK
VMA	19	(Clock)	3	K CLK
BGACK	12	(Clock)	2	L CLK
A0	7	ADDRESS	2	0
A1	29	ADDRESS	2	1
A2	30	ADDRESS	2	2
A3	31	ADDRESS	2	3
A4	32	ADDRESS	2	4
A5	33	ADDRESS	2	5
A6	34	ADDRESS	2	6
A7	35	ADDRESS	2	7
A8	36	ADDRESS	2	8
A9	37	ADDRESS	3	0
A10	38	ADDRESS	3	1
A11	39	ADDRESS	3	2
A12	40	ADDRESS	3	3
A13	41	ADDRESS	3	4
A14	42	ADDRESS	3	5
A15	43	ADDRESS	3	6
A16	44	ADDRESS	3	7
A17	45	ADDRESS	3	8
A18	46	ADDRESS	4	0
A19	47	ADDRESS	4	1
A20	48	ADDRESS	n/c	
A21	50	ADDRESS	n/c	
A22	51	ADDRESS	n/c	
A23	52	ADDRESS	n/c	

Table B-2. 68000 Signal List (Continued)

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
D0	5	DATA	0	0
D1	4	DATA	0	1
D2	3	DATA	0	2
D3	2	DATA	0	3
D4	1	DATA	0	4
D5	64	DATA	0	5
D6	63	DATA	0	6
D7	62	DATA	0	7
D8	61	DATA	1	0
D9	60	DATA	1	1
D10	59	DATA	1	2
D11	58	DATA	1	3
D12	57	DATA	1	4
D13	56	DATA	1	5
D14	55	DATA	1	6
D15	54	DATA	1	7
LR_W	9	STATUS	4	2
LUDS_LLDS	-	STATUS	4	3
VMA	19	STATUS	4	4
FC0	28	STATUS	4	5
FC1	27	STATUS	4	6
FC2	26	STATUS	4	7
BGACK	12	STATUS	4	8

NOTE

The LUDS_LLDS signal is the logical OR of CPU signals $\overline{\text{LUDS}}$ and $\overline{\text{LLDS}}$.

Operation

The logic analyzer will automatically be configured for state analysis when you load the inverse assembler from the digital cassette drive.

Format Specification

When using the 68000 interface module, the format specification will be set up by the mini-cassette software as shown in figure B-3.

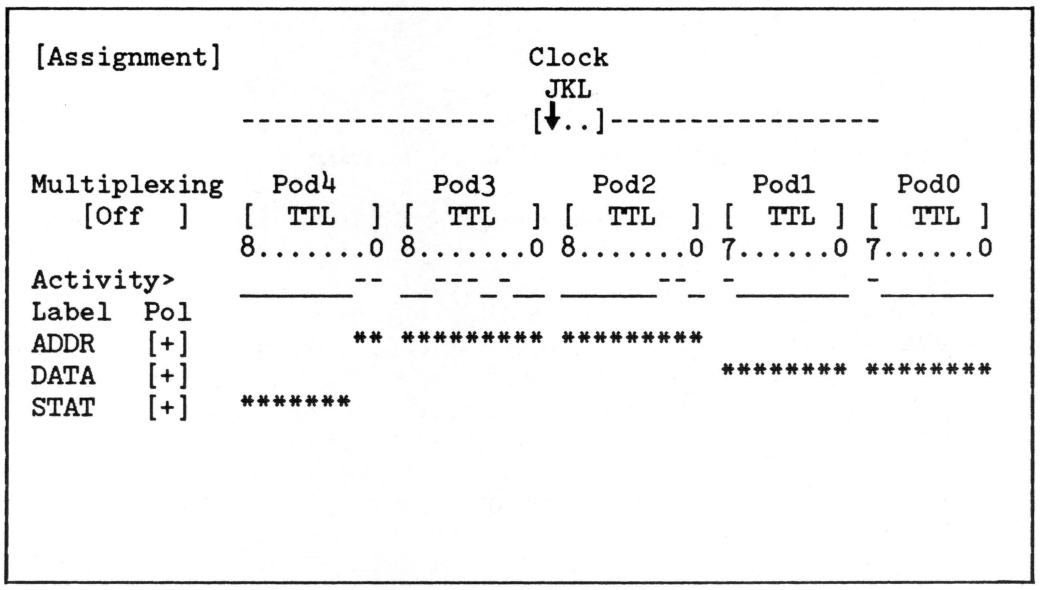

Figure B-3. 68000 Format Specification

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display of the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The signal AS is the master clock to the logic analyzer.

The 68000 Inverse Assembler

The 68000 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. To obtain this display, proceed as follows:

1. Press the RUN key to take a trace. The display will show address and data in hex. The inverse-assembly area will show program reads and writes.

2. On the display, select a bus cycle line that you know is the first word of an instruction (a program read).

3. Roll the selected line to the point where its line number is in the inverse-video box.

4. Press the INSERT key (message at top of screen says INSERT to Inverse-Assemble). All information from the selected line to the bottom of the screen will be inverse assembled. All information preceding the selected line will be unchanged.

If you roll the display toward the end of memory, each new line on screen will be inverse assembled. The analyzer only inverse assembles information on screen.

If you address a new memory location by typing in a new line number in the inverse-video field, the display will not be inverse-assembled. Repeat steps 2 through 4 above to obtain inverse assembly of the new display.

NOTE

> Each time you inverse assemble a block of memory, the analyzer will keep that portion in the inverse-assembled condition. You can inverse assemble several different blocks in the analyzer memory. The activity between those blocks will not be inverse assembled.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an operand was not stored in the logic analyzer memory. Two pairs of asterisks (****) indicate that one word of an expected operand was missing, with four pairs of asterisks signifying a missing long word. Note that missing operands (or parts of operands) can be the result of 68000 instruction prefetch activity, or result from storage qualification.

Examples:

```
ORI.B     #**,D2          (missing byte operand)
ORI.W     #****,D1        (missing word operand)
ORI.L     #234A****,D3    (missing (lower) word of operand)
ORI.L     #********,D3    (missing both words of operand)
```

The 68000 is capable of supporting byte, word, and long word (32 bit) operands. During operand reads and writes, an entire 16 bit (word) value appears on the CPU data bus. In the case of single byte operands, the inverse assembler will display "xx" for the byte of the input data that is ignored by the CPU. In this manner it is possible to determine exactly which byte of data the CPU has used as an operand (as shown below).

Examples:

```
ORI.B     #03,D1
     xx03 supr program read   (CPU uses lower byte
                               only)
ORI.W     #1203,D1
     1203 supr program read   (CPU uses both bytes
                               of word)
```

Error Messages

The following list of messages will help you identify program errors.

Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.

Illegal Opcode - undefined opcode encountered. CPU action is indeterminate.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Appendix C

Interface Module

8085

Introduction

The Model 64655A Processor Interface Module, when installed in the Model 10269A General Purpose Probe Interface, provides a complete interface between any 8085 target system and the Model 1630A/D Logic Analyzer. The interface module connects signals from the 8085 target microprocessor to the logic analyzer inputs, along with all of the status and clock signals required for inverse assembly of the 8085 instruction set.

The 8085 configuration software on the mini-cassette sets up the [Assignment] menu of the logic analyzer format specification for compatibility with the 8085 microprocessor, and assigns names to values found on the 8085 status bus. It also contains the inverse assembler routine required to obtain displays of 8085 data in assembly language mnemonics. The interface module specifications are given in table C-1.

Table C-1. Interface Module Specifications

Processor Compatibility:	Intel 8085 and all microprocessors made by other manufacturers which comply with Intel 8085 specifications.
Maximum Clock Speed:	6 MHz clock output from microprocessor.
Signal Line Loading:	One LS TTL load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.30 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.
Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for state analysis of an 8085 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 055 which includes:

   (1). 64655A Interface Module for 8085 microprocessors, including an 8085 interface circuit card and cable assembly.

   (2). 8085 inverse assembler and Format Specification setups on Minicassette HP Part No. 64655-11001.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

The Model 1630D enables storage of up to 8 additional channels of information.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the 8085 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure C-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure C-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

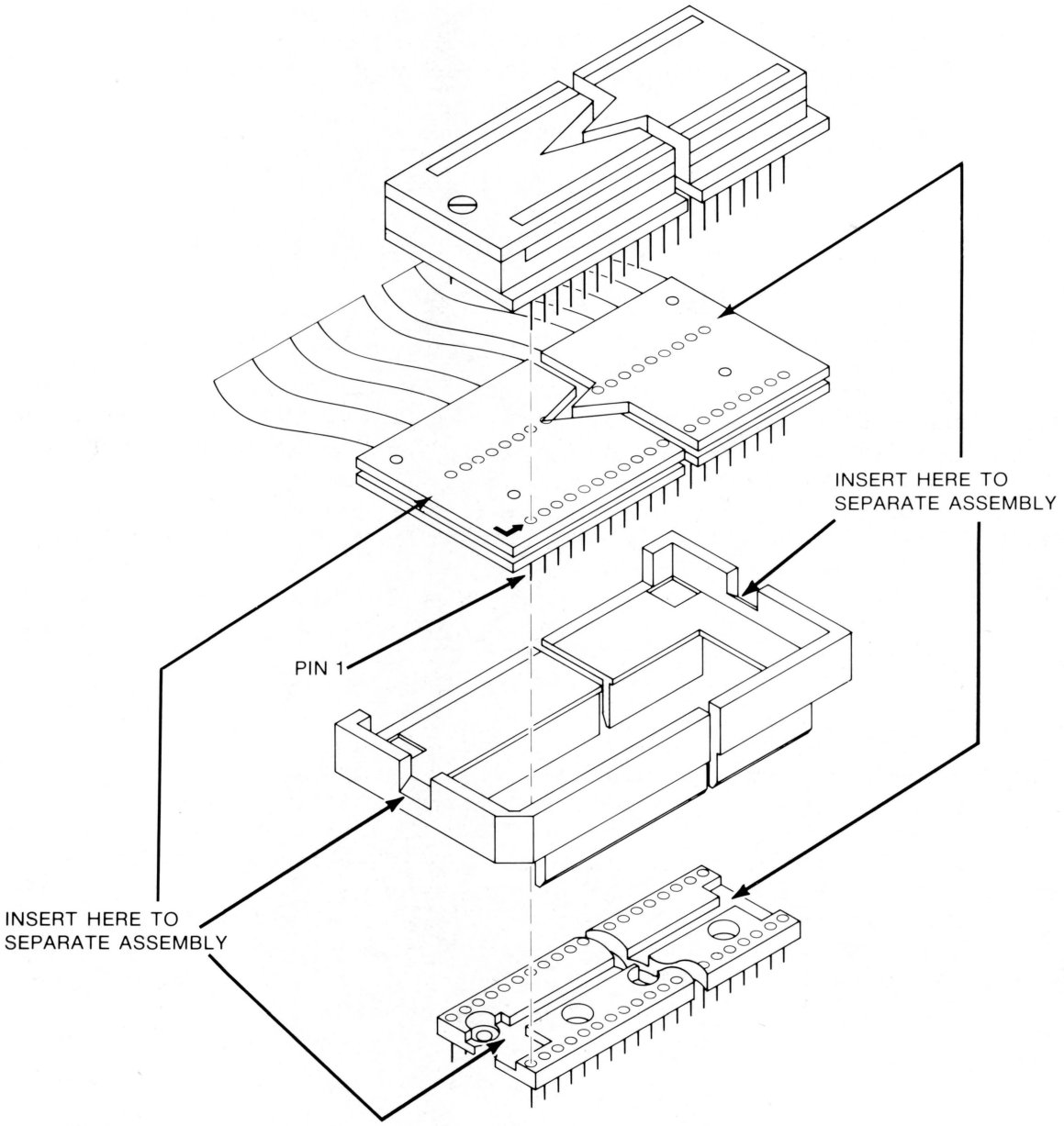

Figure C-1. ZIF Socket Assembly, Exploded View

General Purpose
Probe Interface

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	1
B	4
C	2
D	3
E	n/c

Interface Description

The 8085 interface circuit is comprised of buffers and NAND gates. Generation and gating of some status signals to the general purpose probe interface is performed by the NAND gates. Figure C-2 shows the 8085 interface block diagram.

Table C-2 lists the CPU signals and cable lines on which those signals are carried to the logic analyzer.

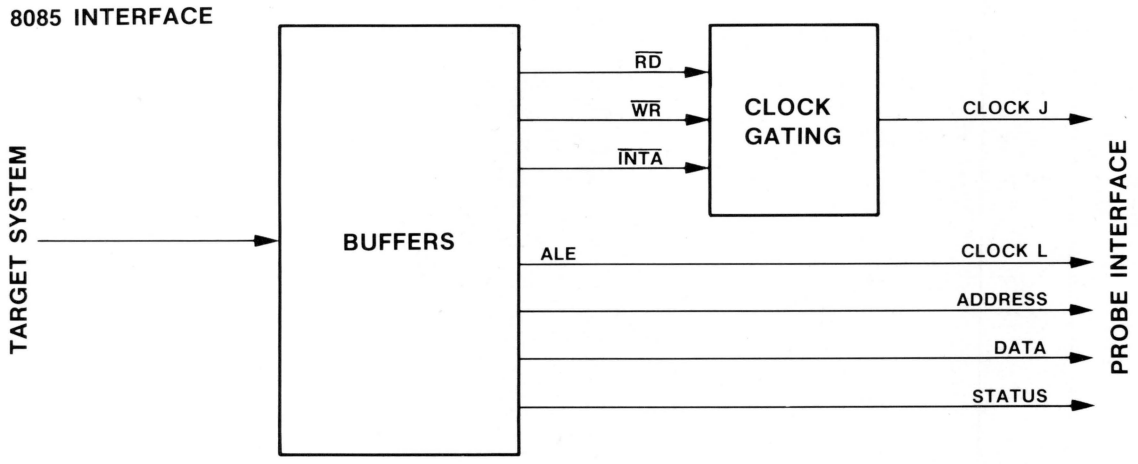

Figure C-2. 8085 Interface Block Diagram

Table C-2. 8085 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	12	ADDRESS	2	0
AD1	13	ADDRESS	2	1
AD2	14	ADDRESS	2	2
AD3	15	ADDRESS	2	3
AD4	16	ADDRESS	2	4
AD5	17	ADDRESS	2	5
AD6	18	ADDRESS	2	6
AD7	19	ADDRESS	2	7
A8	21	ADDRESS	2	8
A9	22	ADDRESS	3	0
A10	23	ADDRESS	3	1
A11	24	ADDRESS	3	2
A12	25	ADDRESS	3	3
A13	26	ADDRESS	3	4
A14	27	ADDRESS	3	5
A15	28	ADDRESS	3	6
SID	5	SID	3	7
SOD	4	SOD	3	8
AD0	12	DATA	1	0
AD1	13	DATA	1	1
AD2	14	DATA	1	2
AD3	15	DATA	1	3
AD4	16	DATA	1	4
AD5	17	DATA	1	5
AD6	18	DATA	1	6
AD7	19	DATA	1	7
S0	29	STATUS	4	0
S1	33	STATUS	4	1
HLDA	38	STATUS	4	2
IO/LM	34	STATUS	4	3
ALE	30		2	L clk
NAND OF:			4	J clk
$\overline{\text{INTA}}$	11			
$\overline{\text{WR}}$	31			
$\overline{\text{RD}}$	32			

Operation

The logic analyzer will be configured for state analysis when you load the inverse assembler from the digital cassette drive.

Format Specification

When using the 8085 interface module, the format specification will be set up by the mini-cassette software as shown in figure C-3.

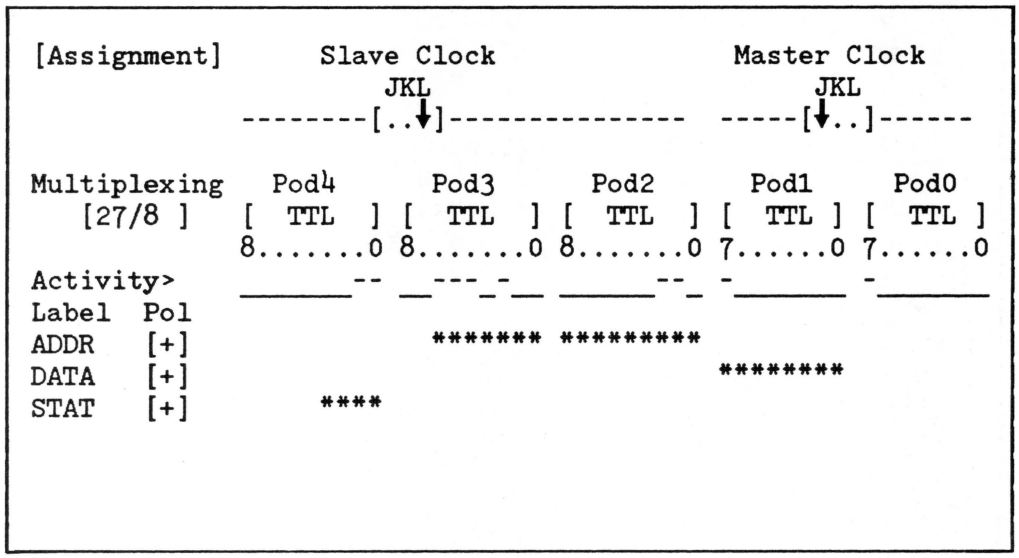

Figure C-3. 8085 Format Specification

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display of the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The logical NAND of CPU signals $\overline{\text{INTA}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ is used as the master clock signal to the logic analyzer.

ALE is used as the slave clock signal to the logic analyzer.

User Base

The User Base menu of the format specification is set up with names to identify values found on the status label. See figure C-4.

State Format Specification

[User Base]

State Labels

Value [BIN]	STAT	
0000		
0001	memwr	(memory_write)
0010	memrd	(memory_read)
0011	opfch	(opcode_fetch)
0100		
0101		
0110		
0111		
1000		
1001	io wr	(I/O_write)
1010	io rd	(I/O_read)
1011	intak	(interrupt_acknowledge)
1100		
1101		
1110		
1111		

Figure C-4. 8085 Status Map

The 8085 Inverse Assembler

The 8085 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that one byte of an expected (single or double byte) operand was not stored in the logic analyzer memory. Two pairs of asterisks (****) indicate that both bytes of a double byte operand were not stored.

If the standard 8085 trace and format specifications (from the 8085 configuration file) are used for making measurements, asterisks will be displayed when a conditional jump or conditional call instruction is evaluated to be false. The number of operand fetches (memory reads) performed is dependent upon the evaluation result.

If the evaluation is true, two operand fetches will produce the address to which program control will be passed. No asterisks will be displayed since both bytes of the operand will be present. If the evaluation is false, only one operand is fetched before control is passed to the next address in sequence. Since one of the two operands is missing, a pair of asterisks will be displayed instead of the (missing) high order byte.

Examples:

JNZ	0357	indicates that since the non-zero (NZ) condition was true, the jump to 0357H will occur.
JNZ	**57	indicates that since the non-zero (NZ) condition was false, the jump will not occur.

In the case that the conditional call or jump occurs at the end of logic analyzer memory, asterisks will be displayed for each byte of the operand not found in logic analyzer memory.

If the standard 8085 trace and format specification is used for a measurement these asterisks provide a convenient method to determine whether or not a conditional call or jump was executed.

In general, asterisks indicate that expected operand fetches are not stored in logic analyzer memory. If the standard 8085 trace and format specifications are not utilized, missing operand fetches can be due to the use of storage qualification.

Error Messages

The following list of messages will aid the user in identifying operation errors.

Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.

Illegal Opcode - undefined opcode encountered. Result is indeterminate.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Appendix D

Interface Module
Z8001/Z8002

Introduction

The Model 64680A Processor Interface Module (Z8001), or the Model 64681A Processor Interface Module (Z8002), with the Model 10269A General Purpose Probe Interface, will provide a complete interface between any Z8001 or Z8002 target system and the Model 1630A/D Logic Analyzer. The interface module connects signals from the Z8001 or Z8002 target microprocessor to the logic analyzer inputs, along with all of the status and clock signals required for inverse assembly of the Z8001/Z8002 instruction set.

Information provided in this appendix is applicable to both interface modules, unless otherwise stated.

The Z8001 or Z8002 configuration software on the mini-cassette sets up the [Assignment] menu of the logic analyzer format specification for compatibility with the Z8001 or Z8002 microprocessor. It also contains the inverse assembler routine required to obtain displays of either the Z8001 or Z8002 data in assembly language mnemonics. The interface module specifications are given in table D-1.

Table D-1. Interface Module Specifications

Processor Compatibility:	Zilog Z8001 and Z8002 and all microprocessors made by other manufacturers which comply with Zilog 8001 or Zilog 8002 specifications.
Maximum Clock Speed:	6 MHz clock input to microprocessor.
Signal Line Loading:	One LS TTL load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.50 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer

Table D-1. Interface Module Specifications (Continued)

Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for state analysis of a Z8001/Z8002 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 080 for Z8001, which includes:

(1). 64680A Interface Module for Z8001 microprocessors, including a Z8001 interface circuit card and cable assembly.

(2). Z8001 inverse assembler and Format Specification setups on Minicassette HP Part No. 64680-11000.

(OR)

b. 10269A General Purpose Probe Interface with Option 081 for Z8002, which includes:

(1). 64681A Interface Module for Z8002 microprocessors, including a Z8002 interface circuit card and cable assembly.

(2). Z8002 inverse assembler and Format Specification setups on Minicassette HP Part No. 64681-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the Z8001/Z8002 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure D-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure D-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

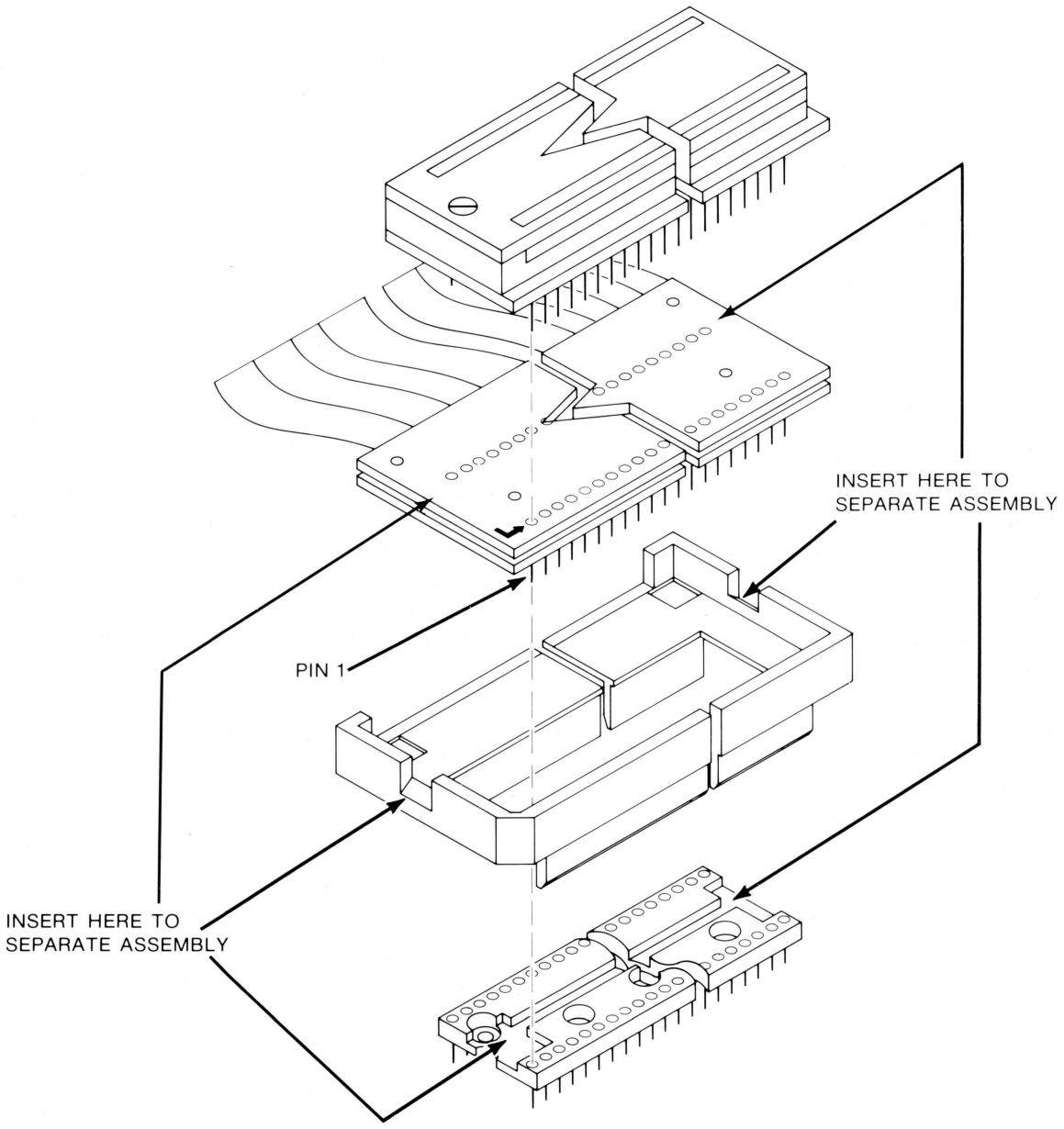

Figure D-1. ZIF Socket Assembly, Exploded View

General Purpose
Probe Interface

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	0
B	1
C	2
D	3
E	4

Interface Description

The Z8001 and Z8002 microprocessors are a multiplexed address/data bus. The 16-bit address appears on the bus at the beginning of a transaction (along with the 7-bit segment number for the Z8001). Later in the transaction, data is either written to, or read from, the bus by the microprocessor. These lines are buffered in the interface module. Address (and segment number for the Z8001) is latched in the logic analyzer when ths address strobe is active (ClocK L). The status lines are also latched with address at the beginning of the cycle. The Z8001 data strobe signal is used to clock all data transactions into the logic analyzer. This signal is inverted and input to the logic analyzer as Clock J. Circuitry on the interface board generates an additional clock for memory refresh cycles only. This signal is input to the logic analyzer as Clock K. Figure D-2 shows the Z8001/Z8002 interface block diagram.

Table D-2 lists the CPU signals and cable lines on which the Z8001 signals are carried to the logic analyzer. Table D-3 lists the CPU signal and cable lines on which the Z8002 signals are carried to the logic analyzer.

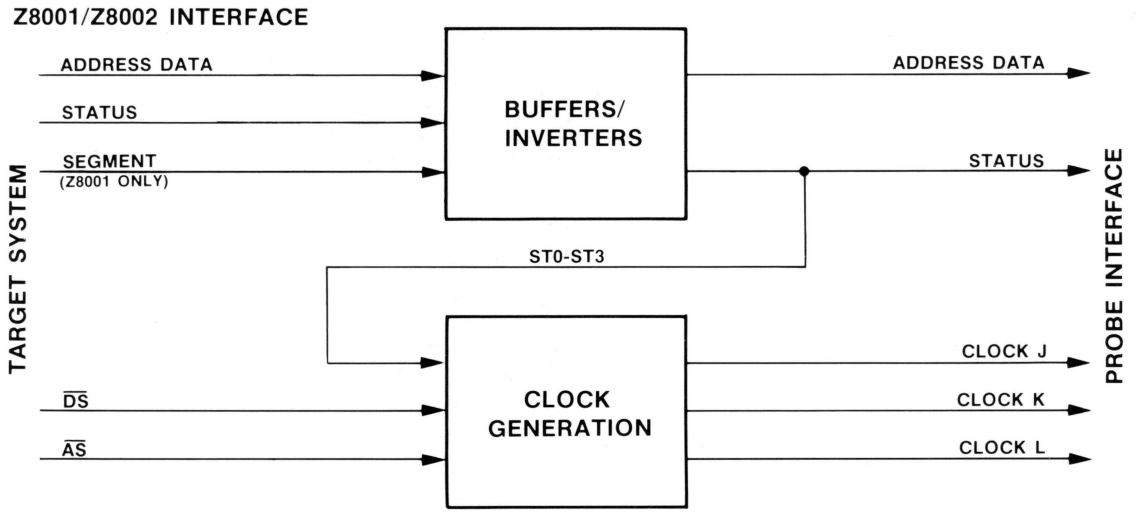

Figure D-2. Z8001/Z8002 Interface Block Diagram

Table D-2. Z8001 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	1	ADDRESS	2	0
AD1	38	ADDRESS	2	1
AD2	39	ADDRESS	2	2
AD3	40	ADDRESS	2	3
AD4	43	ADDRESS	2	4
AD5	41	ADDRESS	2	5
AD6	44	ADDRESS	2	6
AD7	45	ADDRESS	2	7
AD8	48	ADDRESS	2	8
AD9	2	ADDRESS	3	0
AD10	3	ADDRESS	3	1
AD11	4	ADDRESS	3	2
AD12	5	ADDRESS	3	3
AD13	6	ADDRESS	3	4
AD14	10	ADDRESS	3	5
AD15	9	ADDRESS	3	6

Table D-2. Z8001 Signal List (Continued)

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
SN0	26	ADDRESS	3	7
SN1	25	ADDRESS	3	8
SN2	37	ADDRESS	4	0
SN3	24	ADDRESS	4	1
SN4	42	ADDRESS	n/c	
SN5	46	ADDRESS	n/c	
SN6	47	ADDRESS	n/c	
N/LS	31	ADDRESS	n/c	
AD0	1	DATA	0	0
AD1	38	DATA	0	1
AD2	39	DATA	0	2
AD3	40	DATA	0	3
AD4	43	DATA	0	4
AD5	41	DATA	0	5
AD6	44	DATA	0	6
AD7	45	DATA	0	7
AD8	48	DATA	1	0
AD9	2	DATA	1	1
AD10	3	DATA	1	2
AD11	4	DATA	1	3
AD12	5	DATA	1	4
AD13	6	DATA	1	5
AD14	10	DATA	1	6
AD15	9	DATA	1	7
R/LW	30	STATUS	4	2
B/LW	32	STATUS	4	3
N/LS	31	STATUS	4	4
ST0	23	STATUS	4	5
ST1	22	STATUS	4	6
ST2	21	STATUS	4	7
ST3	20	STATUS	4	8
		(Clock)	4	J CLK
		(Clock)	3	K CLK
		(Clock)	2	L CLK

Table D-3. Z8002 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	40	ADDRESS	2	0
AD1	32	ADDRESS	2	1
AD2	33	ADDRESS	2	2
AD3	34	ADDRESS	2	3
AD4	36	ADDRESS	2	4
AD5	35	ADDRESS	2	5
AD6	37	ADDRESS	2	6
AD7	38	ADDRESS	2	7
AD8	39	ADDRESS	2	8
AD9	1	ADDRESS	3	0
AD10	2	ADDRESS	3	1
AD11	3	ADDRESS	3	2
AD12	4	ADDRESS	3	3
AD13	5	ADDRESS	3	4
AD14	9	ADDRESS	3	5
AD15	8	ADDRESS	3	6
R/LW	25		3	7
B/LW	27		3	8
AD0	40		4	0
N/LS	26		4	1
ST0	21		n/c	
ST1	20		n/c	
ST2	19		n/c	
ST3	18		n/c	

Table D-3. Z8002 Signal List (Continued)

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	40	DATA	0	0
AD1	32	DATA	0	1
AD2	33	DATA	0	2
AD3	34	DATA	0	3
AD4	36	DATA	0	4
AD5	35	DATA	0	5
AD6	37	DATA	0	6
AD7	38	DATA	0	7
AD8	39	DATA	1	0
AD9	1	DATA	1	1
AD10	2	DATA	1	2
AD11	3	DATA	1	3
AD12	4	DATA	1	4
AD13	5	DATA	1	5
AD14	9	DATA	1	6
AD15	8	DATA	1	7
R/LW	25	STATUS	4	2
B/LW	27	STATUS	4	3
N/LS	26	STATUS	4	4
ST0	21	STATUS	4	5
ST1	20	STATUS	4	6
ST2	19	STATUS	4	7
ST3	18	STATUS	4	8
		(Clock)	4	J CLK
		(Clock)	3	K CLK
		(Clock)	2	L CLK

Operation

The logic analyzer will be configured for state analysis when you load the inverse assembler from the digital cassette drive.

Z8001 Format Specification

When using the Z8001 interface module, the format specification will be set up by the mini-cassette software as shown in figure D-3.

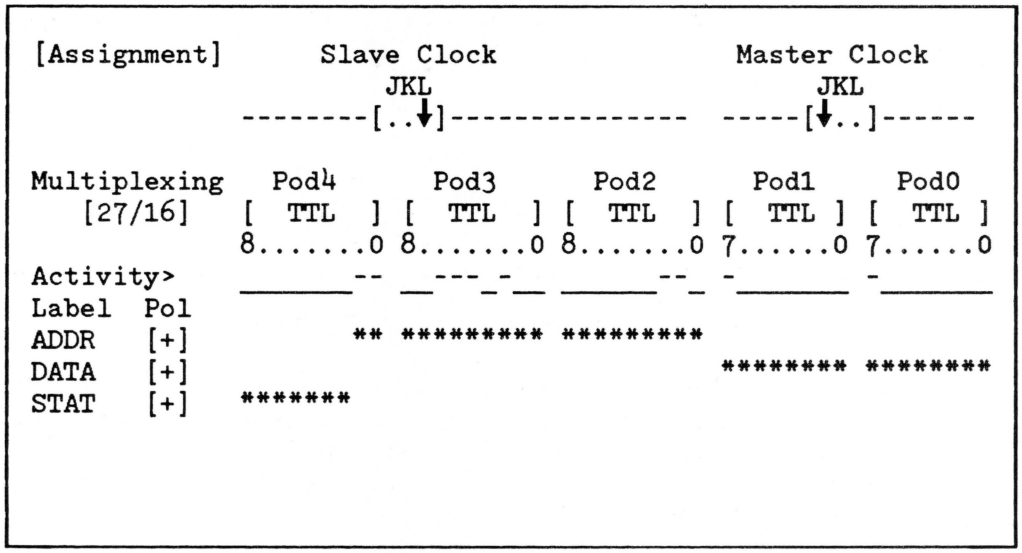

Figure D-3. Z8001 Format Specification

Z8002 Format Specification

When using the Z8002 interface module, the format specification will be set up by the mini-cassette software as shown in figure D-4.

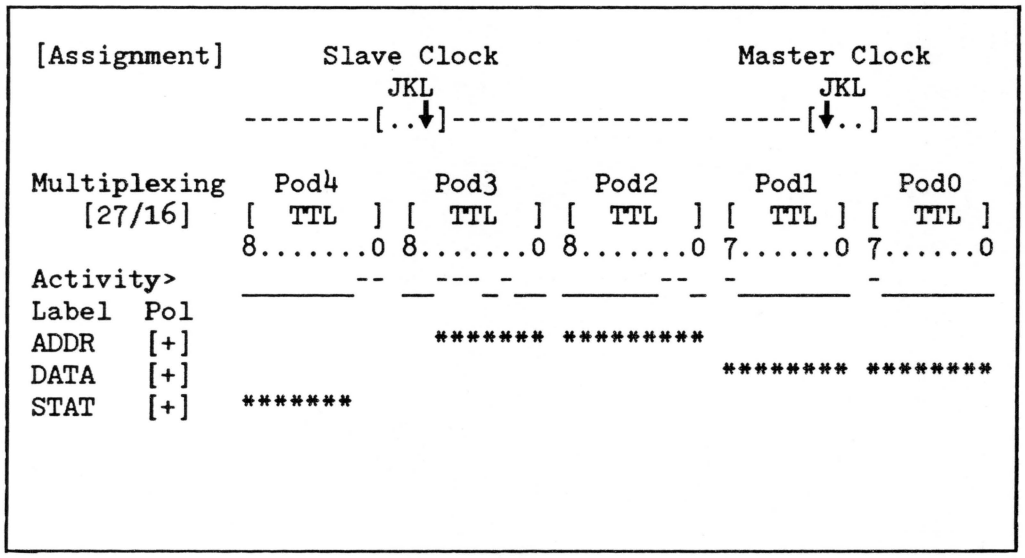

Figure D-4. Z8002 Format Specification

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display of the trace list. Pertinent control and clock threshold levels are also part of the format specification.

Address and status is clocked into the logic analyzer by Clock L. Data is clocked into the logic analyzer by Clock J. LDS, after inversion on the interface circuit card, drives Clock J.

The Z8001/Z8002 Inverse Assembler

The Z8001/Z8002 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an operand was not stored in the logic analyzer memory. Two pairs of asterisks (****) indicate that one word of an expected operand was missing, with four pairs of asterisks (********) signifying a missing long word. Note that missing operands, or missing parts of operands, can be a result of storage qualification.

Examples:

```
LD      ****,R1              (missing word operand)

LD      RR0,#********        (missing both words of
                              operand)
```

The Z8001/Z8002 inverse assembler is capable of supporting byte, word, and long word (32 bit) operands. During operand reads or writes, an entire 16-bit (word) value appears on the CPU data bus. In the case of single byte operands, the inverse assembler will display "xx" for the byte of the input data that is ignored by the CPU. In this manner, it is possible to determine exactly which byte of data the CPU has used as an operand.

Example:

```
INB    RH0,235A
  FFF2 program read
  xx03 i/o read                (low byte transfer)
```

Error Messages

The following list of messages will help you identify operation errors.

Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.

Illegal Opcode - undefined opcode encountered. Result is indeterminate.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Appendix E

Interface Module

8086/8088

Introduction

The Model 64653A Processor Interface Module, with the 10269A General Purpose Probe Interface, provides a complete interface between an 8086 or 8088 target system and the Model 1630A/D Logic Analyzer. The interface module connects the signals from the 8086 or 8088 target CPU to the logic analyzer inputs and generates all status and clock signals required by the software for inverse assembly of the 8086/8088 instruction set. The target system CPU can be operated in either minimum or maximum mode; the interface module automatically configures itself for the proper mode. If the CPU is in maximum mode the interface module can, at the user's option, completely dequeue the instruction stream. As instructions are executed by the CPU, they are sent to the logic analyzer. Any instructions that are prefetched by the CPU but not executed are not sent to the logic analyzer. Any bus cycles made by an 8087 or 8089 coprocessor that shares the local bus with the 8086 or 8088 microprocessor will also be captured by the logic analyzer. The interface module specifications are given in table E-1.

Table E-1. Interface Module Specifications

Processor Compatibility:	Intel 8086 and 8088 and all microprocessors made by other manufacturers which comply with Intel 8086 or 8088 Specifications.
Maximum Clock Speed:	10 MHz clock input to microprocessor.
Signal Line Loading:	CLK input is 2 LS TTL loads plus approx 40 pF capacitance. All other inputs are 1 LS TTL load plus approx 35 pF capacitance.
Power Consumption:	1.0 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.

Table E-1. Interface Module Specifications (Continued)

Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for state analysis of an 8086/8088 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 053 which includes:

(1). 64653A Interface Module for 8086 and 8088 microprocessors, including an 8086/8088 interface circuit card and cable assembly.

(2). 8086/8088 inverse assembler and Format Specification setups on Minicassette HP Part No. 64653-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

The Model 1630D enables storage of up to 8 additional channels of information. Model 1630A cannot be used for analysis of 8086 microprocessors.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the 8086 or 8088 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure E-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure E-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

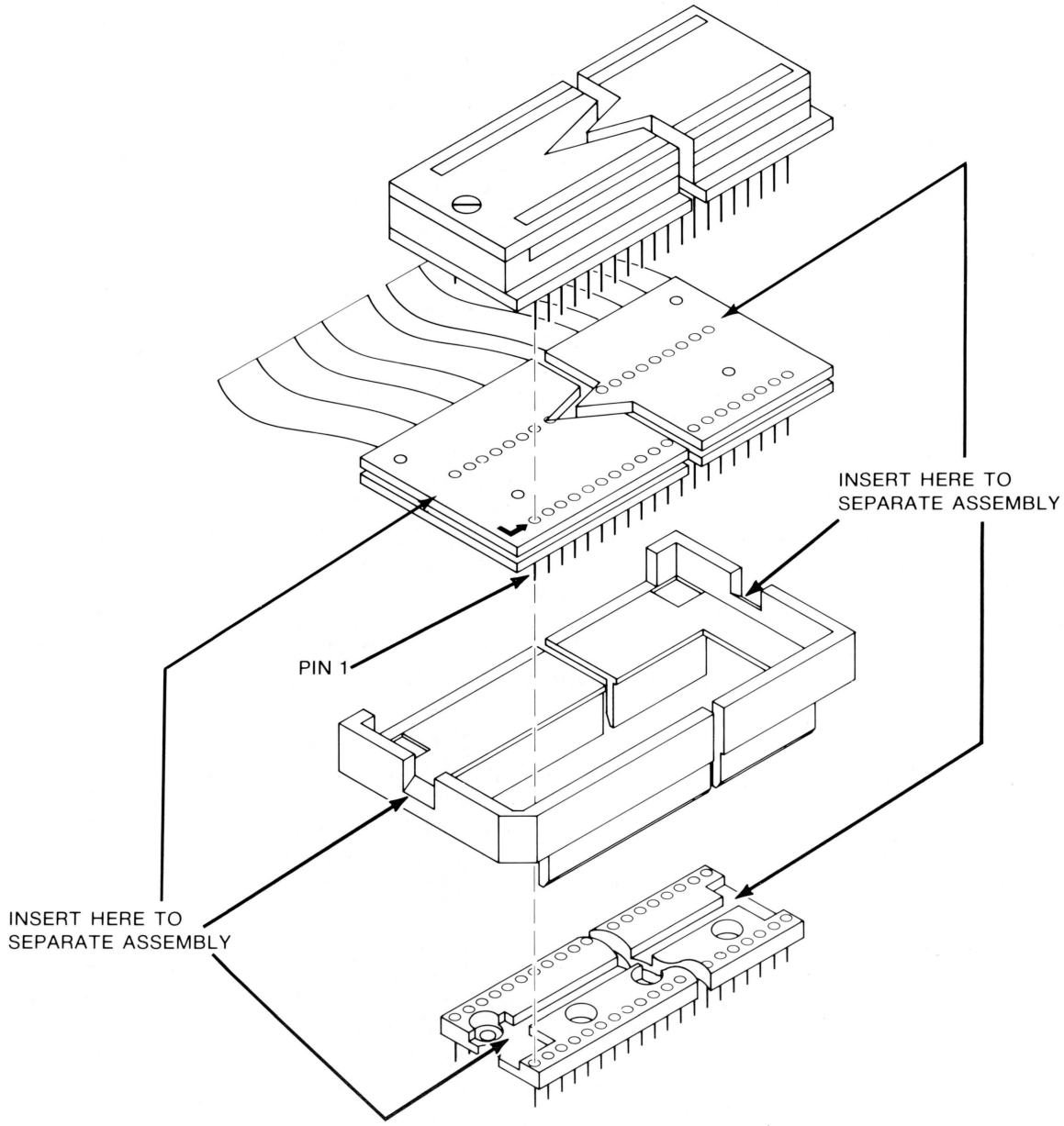

Figure E-1. ZIF Socket Assembly, Exploded View

General Purpose
Probe Interface

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod	
	8086	8088
A	0	1
B	1	n/c
C	2	2
D	3	3
E	4	4

Interface Description

The primary function of the interface module is to connect the target CPU to the logic analyzer through the general purpose probe interface and to perform any required functions that are unique to that particular CPU. There are several functions that are unique to the 64653A 8086/8088 Interface Module. First, the multiplexed address/data bus must be separated so that all information can be sent to the logic analyzer in one state. Second, the status information from the two CPUs is different, and it also varies depending upon whether the CPU is in minimum or maximum mode. The interface module translates the status received from the CPU into a consistent form for the logic analyzer. Third, the interface module duplicates the instruction queue inside the CPU, sending only executed instructions to the logic analyzer when the CPU is in maximum mode. The circuitry of the interface module is described in the following paragraphs; refer to the block diagram in figure E-2.

All information from the CPU is buffered and latched by the Bus Latch on each CPU clock cycle. This latched information is then available to the other sections of the interface module. When the Bus Latch holds the address of a memory or I/O transfer, this information is moved to the Address Latch. When the Bus Latch holds the data from that transfer, the Data Buffer allows that data to be sent to the logic analyzer along with the previously sampled address. The Controller generates status to indicate what kind of transfer was made along with a clock signal for

the logic analyzer. The Controller also generates signals that tell the Address Latch when to accept an address and the Data Buffer when it should allow data to pass through. This process is performed for every bus operation, including instruction fetches, if the CPU is in minimum mode or if the CPU is in maximum mode and the user has selected to not de-queue instructions. If you desire to see only executed instructions, set the BUS/EXECUTED switch (inside the interface module) to the EXECUTED position; the operation will be modified as follows.

In the EXECUTED mode, bus operations that fetch 8086/8088 instructions from memory are not immediately sent to the logic analyzer. Instead, the instructions are input into the Instruction Queue. This queue duplicates the function of the instruction queue that is inside the CPU. When the queue status lines from the CPU indicate that it is executing a byte from its queue, that same byte is pulled from the Instruction Queue on the interface module and sent to the logic analyzer along with an address from the Address Counter. The Controller is completely responsible for controlling the operation of the Instruction Queue and the Address Counter. The Controller identifies which bus operations are CPU instruction fetches and enters them into the Instruction Queue. It also monitors the CPU operation and sends instructions to the logic analyzer as they are executed. When the CPU executes a program transfer instruction, the Controller clears the Instruction Queue and loads a new value into the Address Counter.

While in the EXECUTED mode, bus operations that are not CPU instruction fetches will immediately be sent to the logic analyzer. This includes all bus operations that are performed by a coprocessor that may be sharing the bus with the 8086/8088. One nice result of this instruction dequeueing is that for instructions that cause a bus operation, such as a memory or I/O read or write, the executed instruction will be immediately followed by the resulting bus operation. Priority is always given to executed instructions if an instruction and a bus operation need to be sent to the logic analyzer at the same time. If a conflict does occur, the status will indicate that a bus operation has been lost. This conflict can occur only with a coprocessor, and even then it is a rare event.

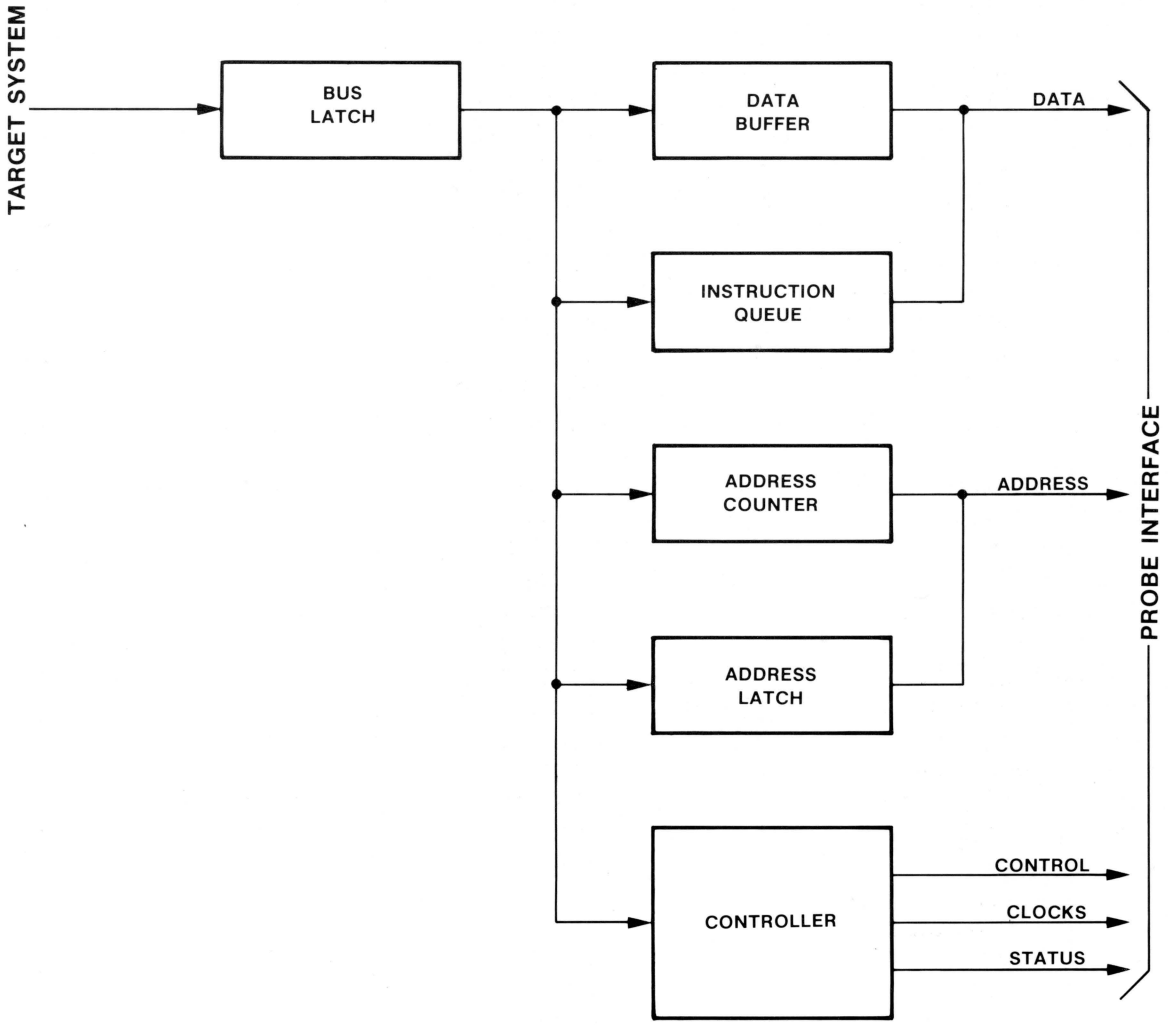

Figure E-2. 8086/8088 Interface Block Diagram

Table E-2 lists the CPU signals and cable lines on which the 8086 signals are input to the logic analyzer.

Table E-2. 8086 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	16	ADDRESS	2	0
AD1	15	ADDRESS	2	1
AD2	14	ADDRESS	2	2
AD3	13	ADDRESS	2	3
AD4	12	ADDRESS	2	4
AD5	11	ADDRESS	2	5
AD6	10	ADDRESS	2	6
AD7	9	ADDRESS	2	7
AD8	8	ADDRESS	2	8
AD9	7	ADDRESS	3	0
AD10	6	ADDRESS	3	1
AD11	5	ADDRESS	3	2
AD12	4	ADDRESS	3	3
AD13	3	ADDRESS	3	4
AD14	2	ADDRESS	3	5
AD15	39	ADDRESS	3	6
A16/S3	38	ADDRESS	3	7
A17/S4	37	ADDRESS	3	8
A18/S5	36	ADDRESS	4	0
A19/S6	35	ADDRESS	4	1
AD0	16	DATA	0	0
AD1	15	DATA	0	1
AD2	14	DATA	0	2
AD3	13	DATA	0	3
AD4	12	DATA	0	4
AD5	11	DATA	0	5
AD6	10	DATA	0	6
AD7	9	DATA	0	7

Table E-2. 8086 Signal List (Continued)

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD8	8	DATA	1	0
AD9	7	DATA	1	1
AD10	6	DATA	1	2
AD11	5	DATA	1	3
AD12	4	DATA	1	4
AD13	3	DATA	1	5
AD14	2	DATA	1	6
AD15	39	DATA	1	7
LS1	27	STATUS	4	2
LBHE/S7	34	STATUS	4	3
LS0	26	STATUS	4	4
LS2	28	STATUS	4	5
A18/S5	36	STATUS	4	6
A19/S6	35	STATUS	4	7
(NOTE 1)		STATUS	4	8

Note 1. This signal is a combination of several CPU signals.

Table E-3 lists the CPU signals and cable lines on which the 8088 signals are input to the logic analyzer.

Table E-3. 8088 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
AD0	16	ADDRESS	2	0
AD1	15	ADDRESS	2	1
AD2	14	ADDRESS	2	2
AD3	13	ADDRESS	2	3
AD4	12	ADDRESS	2	4
AD5	11	ADDRESS	2	5
AD6	10	ADDRESS	2	6
AD7	9	ADDRESS	2	7
A8	8	ADDRESS	2	8
A9	7	ADDRESS	3	0
A10	6	ADDRESS	3	1
A11	5	ADDRESS	3	2
A12	4	ADDRESS	3	3
A13	3	ADDRESS	3	4
A14	2	ADDRESS	3	5
A15	39	ADDRESS	3	6
A16/S3	38	ADDRESS	3	7
A17/S4	37	ADDRESS	3	8
A18/S5	36	ADDRESS	4	0
A19/S6	35	ADDRESS	4	1
AD0	16	DATA	1	0
AD1	15	DATA	1	1
AD2	14	DATA	1	2
AD3	13	DATA	1	3
AD4	12	DATA	1	4
AD5	11	DATA	1	5
AD6	10	DATA	1	6
AD7	9	DATA	1	7
LS1	27	STATUS	4	2
LBHE/S7	34	STATUS	4	3
LS0	26	STATUS	4	4
LS2	28	STATUS	4	5
A18/S5	36	STATUS	4	6
A19/S6	35	STATUS	4	7
(NOTE 1)		STATUS	4	8

Note 1. This signal is a combination of several CPU signals.

Operation

8086/8088 Selection

The 64653A Interface is capable of connecting either the 8086 or the 8088 CPU to the logic analyzer. This is possible because the two CPUs are so similar. A 16-bit versus an 8-bit data bus and the method of encoding minimum mode status are the primary differences between the two CPUs. Be sure switch S1 on the interface module is set for the correct CPU (either 8086 or 8088).

Min/Max Mode

Both the 8086 and the 8088 can operate in either the minimum or the maximum mode of operation. The two modes differ in what status information is available from the CPU and how it is encoded. The 64653A Interface Module detects which mode the CPU is in and automatically adjusts itself for the proper mode of operation. The primary difference in operation of the interface module for the two CPU modes is that the executed instruction mode (dequeued) is only available if the CPU is in max mode. This is because the CPU only provides status about its internal instruction queue when it is in max mode. If the CPU is in min mode, the position of the BUS/EXECUTED switch on the interface module has no effect; only bus cycles will be sent to the logic analyzer.

The second effect that the CPU mode has on the operation of the interface module concerns the generation of status. When either the 8086 or the 8088 is in min mode, the interface module generates max mode style status on the S0 thru S2 lines. For the 8088 this is a simple regrouping of the available status lines. For the 8086 in min mode, however, there is insufficient information. In this mode, it is not possible to determine precisely when the CPU is fetching instructions; the status is the same as a data memory read. The best guess as to when the CPU is fetching instructions is when it is reading from memory using the code segment register. The only time when this assumption will be in error is when a code segment override is performed during a data read. This possible error in the status can occur only when the 8086 is in min mode.

Bus Cycle Mode (fetched instructions)

While the interface module is in this mode of operation all transactions that occur on the bus by both the CPU and coprocessors will be sent to the logic analyzer as they occur. No distinction is made between instructions that are executed and those that are only prefetched by the CPU. There will typically be a several state separation between a memory or I/O read or write and the instruction that caused the transfer. The interface module sends bus transactions to the logic analyzer in the order that they occur and the time count will be an accurate reflection of when they occurred. The logic analyzer is actually clocked on the falling edge of the CPU input clock during the CPU T4 cycle. The bus cycle mode is the only mode available if the CPU is in min mode.

Executed Instruction Mode (dequeued)

This mode of operation of the interface module provides several advantages over the bus cycle mode when tracing program flow. The most important difference is that only executed instructions are sent to the logic analzyer. Any instructions that are fetched but not executed because of a program transfer are not sent to the logic analyzer and therefore do not complicate the trace list. By using the time count feature, the precise execution time of a program segment or loop can be established.

Also, any instruction, even if it starts at an odd address, can be used as a trigger or other event in the trace specification. Normally, instructions are fetched only from even addresses unless a program transfer is made to an odd address. This makes defining the trace specification difficult if the instruction of interest is at an odd address. While in this mode, however, each executed byte of code is sent to the logic analyzer with its address, separately.

Another result of this dequeued mode of operation is that any instruction that causes a memory or I/O read or write will be immediately followed by that transfer. The trace list is an accurate representation of the order in which instructions are executed. The CPU pulls instructions from its queue one at a time and executes them completely, including resultant bus cycles, before executing the next instruction. This logical ordering of instructions and data transfers further reduces the possible confusion in interpreting a tracelist.

Status Encoding

The description of each of the seven bits in the STATUS label is given below. Table E-4 lists the precise value of each bit for all types of cycles that can occur for the 8086 or 8088 CPU and the 8087 and 8089 coprocessors. It should be noted that when the CPU is in min mode, the interface module generates status on the S0 thru S2 lines that looks like max mode status.

POD 4, Bit 2 is the CPU status bit S1.

POD 4, Bit 3 for the 8086 indicates whether a transfer was made on the high byte of the data bus. For the 8088 this bit is the status bit SS0 in min mode or always high in max mode.

POD 4, Bit 4 is the CPU status bit S0.

POD 4, Bit 5 is the CPU status bit S2.

POD 4, Bit 6 during executed bytes indicates if it is the first or next executed byte. During bus cycles it is the CPU status bit S5 and indicates if the CPU interrupt enable flag is set or which coprocessor is the bus master.

POD 4, Bit 7 is the CPU status bit S6 and indicates whether the 8086/8088 or a coprocessor is the current bus master.

POD 4, Bit 8 is used to indicate that a byte of code was executed when a bus cycle occured and the bus cycle was not sent to the logic analyzer.

Table E-4. STATUS Field Encoding

8086 or 8088 CYCLES	label STATUS (Pod 4, Bits) 8	7	6	5	4	3	2
	-	-	-	-	-	-	-
Interrupt Acknowledge	1	0	x	0	0	x	0
Write I/O port	1	0	x	0	0	x	1
Read I/O port	1	0	x	0	1	x	0
Halt Acknowledge	1	0	x	0	1	x	1
Code fetch (not executed)	1	0	x	1	0	x	0
Write memory	1	0	x	1	0	x	1
Read memory	1	0	x	1	1	x	0
Executed first byte of instruction	0	0	0	1	1	1	1
Executed next byte of instruction	0	0	1	1	1	1	1
Executed first byte, lost bus cycle	1	0	0	1	1	1	1
Executed next byte, lost bus cycle	1	0	1	1	1	1	1
Interrupt disabled (see note below)	1	0	0	a	a	x	a
Interrupt enabled (see note below)	1	0	1	a	a	x	a

NOTE: One or more bits labeled "a" must be low, indicating that the cycle is not an executed byte.

8086 BUS CYCLES or 8087 or 8089 CYCLES	label STATUS						
	-	-	-	-	-	-	-
Word transfer (A0 = 0)	1	x	x	x	x	0	x
High byte transfer (A0 = 1)	1	x	x	x	x	0	x
Low byte transfer (A0 = 0)	1	x	x	x	x	1	x

8089 CYCLES	label STATUS						
	-	-	-	-	-	-	-
Code access - I/O space	1	1	1	0	0	x	0
Write I/O port	1	1	1	0	0	x	1
Read I/O port	1	1	1	0	1	x	0
Code access - system memory	1	1	1	1	0	x	0
Write memory	1	1	1	1	0	x	1
Read memory	1	1	1	1	1	x	0

8087 CYCLES	label STATUS						
	-	-	-	-	-	-	-
Write memory	1	1	0	1	0	x	1
Read memory	1	1	0	1	1	x	0

8086 Format Specification

When using the 8086 interface module, the format specification will be set up by the mini-cassette software as shown in figure E-3.

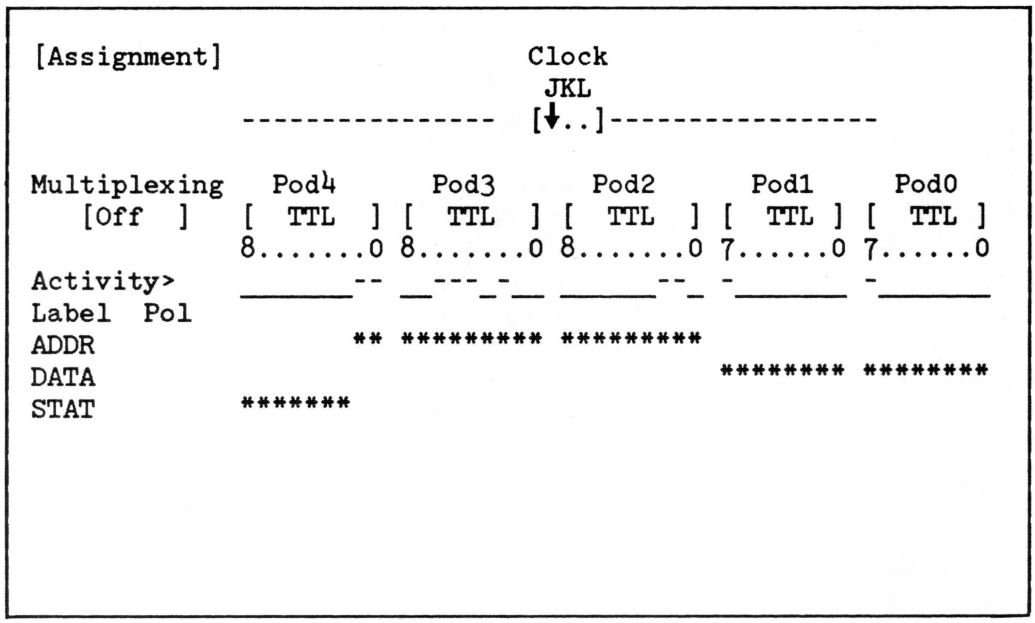

Figure E-3. 8086 Format Specification

8088 Format Specification

When using the 8088 interface module, the format specification will be set up by the mini-cassette software as shown in figure E-4.

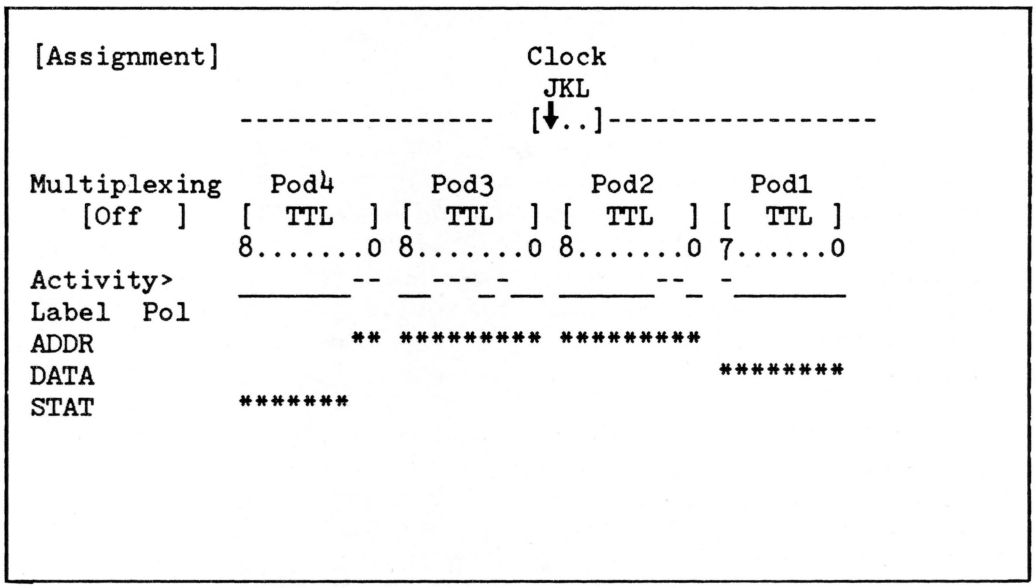

Figure E-4. 8088 Format Specification

Appendix F

Model 10269A Options For Making A User Definable Interface

Introduction

The Model 10269A General Purpose Probe Interface Options provide a means for you to customize an interface module for your Model 10269A General Purpose Probe Interface. Use this appendix as a guide for the design and construction of your custom interface module. The interface module will provide dedicated interconnections between your target system and the logic analyzer. The interface module that you will make can consist of either one of two basic options, and either one of these options may use one of three cable assembly options. The options available are listed below:

Model 10269A, Option 100...Wire Wrapping Interface Module
Model 10269A, Option 101...Microprocessor Interface Kit
Model 10269A, Option 102...40-Pin Cable Assembly
Model 10269A, Option 103...48-Pin Cable Assembly
Model 10269A, Option 104...64-Pin Cable Assembly

No active circuitry is supplied with either of the two basic options (options 100 and 101). If you need active circuitry to generate clocks or status signals, that circuitry can also be located on the interface module, as supplied and defined by the user.

The Wire Wrapping Interface Module provides the user with the basic material with which a custom interface may be built. The necessary circuit board, connectors, and wiring pins that are required for a simple interface are supplied with this option. The Microprocessor Interface Kit provides additional components, such as sockets, capacitors, and more wiring pins and connectors. These additional components are used to support active circuitry that may be required on the interface board. The cable assembly options are probe cables that can be used to probe dual in-line style packages.

The specifications of the user definable interface module are listed in table F-1. The specifications for the clock and data inputs define limits of the logic analyzer/probe interface system and the environment in which the interface module must be designed. Many of the clock and data inputs specifications can be affected by the interface module design. The load on the system is determined by any circuitry you place on the interface module. The setup and hold times of the information channels are also affected. These times will increase if simple buffers are used on the interface module. The setup and hold times may decrease if latches or flip flops are used to sample information on the interface module. All specifications, other than the clock and data inputs, are established by the design of the interface module.

Understanding The Target System

The primary requirement for design of an interface module is a complete understanding of the target system. You must know what information is to be monitored, when it is valid, and how it can be connected. When the target system is a microprocessor, address, data, and status information must be supplied to the logic analyzer. If the target system is a group of backplane signals or some other digital system, the requirements for interface to the logic analyzer will probably be similar to that of a microprocessor. On an algorithmic state machine, for example, the current state, current inputs and outputs, and the next state will be of interest. Often, you will design the interface module to accommodate the pinout of an interconnect cable. In this case, there will be no active components on the board, only wiring from the target system connector to the pods of the logic analyzer. The following paragraphs will give enough information to allow design of an interface module for connection to any type of system. However, emphasis will be given to interfacing to a microprocessor.

Table F-1. Interface Module Specifications

Clock and Data Inputs

Channel width:	43 data channels (1630D), 35 data channels (1630A), 3 clock channels.
Input impedance:	100 kilohm and <20 pF.
Maximum input:	+/- 40 Vdc.
Dynamic range:	Threshold +/- 10 Vdc.
Minimum signal swing:	600 mV.
Single phase clock pulse rate:	25 MHz maximum with single clock and single edge specified. 20 MHz with any ORed combination of clocks and edges.
Multiplexed clock pulse rate:	Master-Slave clock timing; Master clock must follow slave clock by at least 10 ns and precede next slave clock by 50 ns or more.
Minimum clock pulse width:	10 ns.

Setup and Hold Times

Setup time relative to analysis clock:	>=20 ns.
Hold time relative to analysis clock:	=<0 ns.

Table F-1. Interface Module Specifications (Cont'd)

Power Requirements

Power available to the
interface module: 1.0 A max at +5 +/- 0.25 Vdc.

NOTE: Above power is supplied by the logic analyzer. The interface module may also receive power from the target system or an external supply.

Environment

Temperature: Operating, 0° to 55° C (+32° to +131° F);
Nonoperating, -40° to +75° C (-40° to +167° F).
Altitude: Operating, 4600 m (15,000 ft);
Nonoperating, 15,300 m (50,000 ft).
Humidity: Operating, to 90% noncondensing. Avoid sudden, extreme temperature changes that could cause condensation within the instrument.

Bus Structure

Bus structure, as it applies here, means how the sampled information is grouped together and when it is valid. If the target system is a microprocessor, determine whether it multiplexes address and data on the same lines. If so, the address must be sampled and held in the analyzer until data and any other information can be captured, simultaneously. See if a separate bus is used for I/O transfers. If separate buses are used at different times, maybe the interface module can combine the information and thereby reduce the number of analysis channels needed, still allowing both buses to be monitored.

Clock Characteristics

A signal to clock the logic analyzer will have to be supplied by the target system or generated on the interface module. Determine which signals in the target system indicate when information is transferred. If a bus is multiplexed, there should be a signal to indicate when each piece of information is valid. For example, the 8085 microprocessor has a signal (ALE) to indicate when address is valid on the address/data bus. Many microprocessors use several signals to indicate when different types of data transfers are being made. The 8085 uses three signals to control data transfers: $\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$. You may want to combine these signals into one clock for the logic analyzer. The multiple clock fields of the analyzer may be used to OR several signals to generate a clock.

Status Information

Status generally defines the type of information transfer being made, such as opcode fetch, memory read, I/O write, etc. It is helpful to have as much status information as possible about the kind of state being acquired by the logic analyzer. Status can be used to trigger or store qualify the analyzer or to simply show what is happening in the target system. If your target system does not provide enough status information, you may want to implement a circuit on the interface module that will generate or translate the status into a more suitable form. For example, the 6800 microprocessor does not have a status line to indicate which read operations are opcode fetches. You can design an algorithmic state machine to follow along with the 6800, monitoring address, data, $\overline{\text{RESET}}$, R/$\overline{\text{W}}$, and VMA to indicate opcode fetches.

DMA or Multi-Master Operation

If more than one device controls the bus in the target system, you may want to see data transfers from all bus masters. This may be as simple as a single status bit that indicates the bus controller for a given transfer, such as when the microprocessor and DMA controller share a local bus. It may require multiplexing two or more buses together and gating several clock signals together if the microprocessor and DMA controller have separate buses.

Interrupt Structure

Microprocessor interrupts often cause a bus cycle to fetch a vector or interrupt type. You may want the logic analyzer to see these bus cycles. Usually a separate control signal from the microprocessor will control this transfer and it can be used as a clock to send these bus cycles to the analyzer. For other systems, it may be more complex.

Operating Voltage Levels

The operating voltage levels dictate the type of circuitry to be used on the interface module. If no circuitry is on the interface module and signals are input directly to the 1630A/D, the thresholds may be adjusted from -10 to +10 volts. For circuitry on the interface module, only +5V is provided in the general purpose probe interface; if any other voltages are required, they must be supplied from an external source. Refer to the Power Supply Distribution paragraphs in this appendix.

Mechanics of Probing

The primary method of bringing signals onto the interface module is through flat ribbon cables. Several cables can be used to input information to the module; the largest cable can be up to 64 conductors wide. If the target device is a microprocessor or other dual, in-line package, there are optional cable assemblies for the user-definable interface that may make this connection easier (refer to the end of this appendix for information about optional cable assemblies). You may want to design into the target system an analysis port for testing and service.

Understanding The Interface Module

The signals that need to be connected through the interface module and general purpose probe interface to the logic analyzer are divided into groups and described in the following paragraphs.

For ease of connection, the instructions in this appendix are written for the following Logic Analyzer/Probe Interface connections:

Model 10269A Connector	Model 1630A/D Pod
A	0 (1630D only)
B	1
C	2
D	3
E	4

Clock Inputs

The 1630A/D Logic Analyzer has three clock inputs lettered J, K, and L. All three clock channels are connected through the interface module. The signal threshold of these lines may be varied along with the thresholds selected for the associated information channels. The signal ground reference for the clock channels is also available on the printed circuit board.

State Data Inputs

The 1630A Logic Analyzer can receive up to 35 channels; the 1630D up to 43 channels. All channels can come through the interface module and the general purpose probe interface. The channels are separated into three groups labeled Pod1 through Pod3 on the printed circuit board. Table F-4 lists the interconnections to be made between pins in the POD and CLOCK groups on the printed circuit board and pins in the interface module buckets labeled A through E. The signal thresholds of all channels may be varied in each pod group from +10 volts to -10 volts in 0.1-volt increments. The ground reference is also available for each pod group. It must be connected to the ground reference of the devices that are driving the associated channels.

Signal Buffering

The main reason for using buffers on the interface module is to reduce loading of signals in the target system. For example, if the microprocessor has a multiplexed address/data bus, each line of the bus will need to be monitored for address and also for data. Where clock signals and status lines are used to drive several inputs, double probing may be done on the interface module. Buffering will substantially reduce the load on the target system lines.

In addition to resistive loading, another reason to buffer signals on the interface module is capacitive loading. Most microprocessors are specified for a maximum capacitive load of 100 pF in order to maintain all propagation delays. The capacitive load of the optional probe cable is 20 to 25 pF, and the input capacitance of most TTL buffers is 7 to 10 pF. Therefore, if the buffers are placed near the left side of the interface board so the wiring capacitance is small, the total load capacitance will be 30 to 35 pF. This load will probably be small enough to present no problem. However, if buffers are not placed on the interface board and the inputs are routed directly into the general purpose probe interface, the load capacitance will be much greater. The input capacitance of the 10269A is 20 pF, and wiring capacitance across the interface board will add another 20 pF or so. This, combined with the cable capacitance, yields 60 to 65 pF. Depending on the load that exists on the target system board, this additional load may be unacceptable.

If buffers are used on the board, select a type that is compatible with the circuitry in the target system. Often the target system is TTL or TTL-compatible. In this case, the 74LS240 family of parts often work well. If the target system is ECL, then an ECL buffer will be required and proper termination will probably be necessary because of cable length. In general, use the same type of buffer that is used in the target system on the interface module.

Setup And Hold Times

Include setup and hold times in your design to be sure information will be acquired correctly by the logic analyzer. The design of the interface module must guarantee that the setup and hold times of the logic analyzer will be satisfied by the target system. Assume that the microprocessor or target system does not multiplex address and data on the same lines; all information is valid at the same time. One design is to place buffers on the interface board for all data and clock lines. The input specifications in table F-1 show 20-ns setup and 0-ns hold times at the general purpose probe interface. Assume the same type of buffers are used on the interface module for the clock and data lines and that they have a minimum propagation delay of 5 ns and a maximum delay of 15 ns. The following equations calculate the setup and hold times that the target system must satisfy at the interface module input:

```
required setup time = analyzer setup time +
                      maximum buffer prop delay for data path -
                      minimum buffer prop delay for clock path
                    =  20 + 15 - 5
                    =  30 ns

 required hold time = analyzer hold time +
                      maximum buffer prop delay for clock path -
                      minimum buffer prop delay for data path
                    =  0 + 15 - 5
                    =  10 ns
```

This illustrates one disadvantage of placing buffers on the interface module: differential propagation delays will increase the setup and hold times required of the target system.

If buffers are needed on the interface module, but their use will cause unacceptable setup and hold times, one solution is to use faster buffers. Another is to use buffers with smaller differential delays. In some cases the 20-ns setup and 0-ns hold times of the logic analyzer may not be adequate. This may be the case when monitoring the faster clock frequency versions of a microprocessor. The solution to this problem is to use flip flops or latches to capture the information on the interface module. Then send the information to the logic analyzer with a clock generated on the interface module.

Using the 1630A/D to Demultiplex

If the target system uses a multiplexed address/data bus, the address will typically be available on the bus early in the bus cycle, followed later by data. Since it is desirable to have address, data, and status information shown in the same analyzer state, the address must be sampled and held until the data is available. There are at least three ways to solve this problem. The first is to use the slave clock of the logic analyzer to sample the address information and the master clock to sample the data and status. The second is to probe the target system at

a point where the information has already been demultiplexed, if possible. The third is to design latches on the interface module to capture and hold the address information until the remaining information is available.

The 8085 microprocessor has a multiplexed address/data bus where the 16-bit address is first provided along with a signal called ALE (address latch enable) to indicate when address is valid. Later in the bus cycle, 8 bits or data is either written to or read from the lower 8 bits of the same bus. The data transfer is controlled by either $\overline{RD}$ (read), $\overline{WR}$ (write), or $\overline{INTA}$ (interrupt acknowledge).

Since all 18 bits of Pod2 and Pod3 can be latched by the slave clock, the 16-bit address bus will be input as the lower 16 bits of this group and ALE will be used as the slave clock. The lower eight bits of the bus will also need to be input on pod 1 for data. You may place an OR circuit on the interface module to use $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ as the master clock.

Since eight of the bus lines must be double probed, it will probably be desirable to buffer the signals (refer to the preceding paragraphs for buffering). Assume that 74LS241 non-inverting buffers are used and that they have a minimum propagation delay of 8 ns and a maximum delay of 18 ns.

The ALE signal from the 8085 is an active high signal; address is valid at the falling edge of ALE. According to the data sheet for a 5-MHz 8085, address is valid 50 ns before the falling edge of ALE and remains valid for 50 ns after. The falling edge of ALE can thus be used as the slave clock for the logic analyzer.

The next step is to verify that all requirements including setup and hold times will be satisfied. The specifications in table F-1 show the minimum width of the clock signal is 10 ns. From the 8085 data sheet, the minimum width of the ALE signal is 80 ns. Data setup time to the latches in the logic analyzer must be at least 20 ns relative to the active edge of the clock signal. The hold time is 0 ns minimum. The following equations illustrate how to determine whether the interface design will satisfy these requirements.

```
required setup time = 1630A/D setup time +
                      maximum 74LS241 delay for address -
                      minimum 74LS241 delay for ALE
                    =  20 + 18 - 8
                    =  30 ns

required hold time = 1630A/D hold time +
                     maximum 74LS241 delay for ALE -
                     minimum 74LS241 delay for address
                   =  0 + 18 - 8
                   =  10 ns
```

The preceding calculations and the specifications stated earlier for the 8085 guarantee that the logic analyzer will correctly capture address information.

Building the Interface Module

Having completed the design of the interface module the actual hardware must now be fabricated. The following sections contain the information necessary to accomplish this task. The fabrication details are divided into several sections, starting with a description of the components of the interface module and proceeding through actual assembly and initial power up.

Components

In order to fabricate an interface module it is necessary that the user select, install, and interconnect the appropriate component parts on the user-definable interface 64651-26501 Printed Circuit Board. The first part of this section describes all of the components that are supplied with the Wire Wrapping Interface Module and how to load them. The second part describes the components supplied with the Microprocessor Interface Kit. The third part discusses the components that the user must supply to complete a typical interface module.

Wave Soldering the PC Board

The interface module printed circuit board may be wave soldered, if desired, after all components to be soldered are placed on the board. If this is done, some holes on the board should be masked to prevent their filling with solder. This should be done before components are loaded on the board. The holes that should be masked are the four standoff mounting holes (one located at each corner of the board), any pads in the J1 or J2 connector areas that are not used, and the ten power routing holes at the lower left corner of the board. If there are any other parts that will not be loaded on the board, the holes for those parts should also be masked off. Proceed with the assembly through this section; the board will then be ready for soldering.

Components Supplied with the Wire Wrapping Interface Module

The components supplied with the Wire Wrapping Interface Module are the basic parts required to build a very simple interface. Figure F-1 shows a component side view of the printed circuit board with item numbers for all of the parts that are included in the Wire Wrapping Interface Module. Table F-2 lists the component parts with their item number, description, HP part number, and quantity. The following paragraphs, together with figure F-1 and table F-2, will describe how to load each part.

Table F-2. Wire Wrapping Interface Module Components

Item #	Description	HP Part #	Quantity
1	CONN-HEADER 40-PIN	1251-3004	2
2	CONN-POST TYPE 25-PIN	1251-4773	4
3	CONN-POST TYPE 11-PIN	1251-7950	6
4	CONN-POST TYPE 5-PIN	1251-5395	2
5	CONN-HEADER 60-PIN	1251-7575	2

Printed Circuit Card. The 64651-26501 printed circuit card is provided in an unloaded form. It is a four-layer printed circuit card. The component side outer layer is dedicated completely to labelling and indicating where various component parts are loaded and what the function is of the wiring pins. One of the inner layers is a power ground plane for any circuitry of the board. The second inner layer and the circuit side outer layer have traces which connect the wiring pins and connectors together appropriately and provide a power distribution system.

Wiring Pins. The wiring pins that are provided allow the user to make wire wrap style connections between the various sections of the interface module. All the wiring pins have a similar style but vary in the number of pins.

The 5-pin strips, item 4, connect to the eight clock channels and their signal ground. These signals are towards the lower right corner of the board next to J3.

The 11-pin strips, item 3, are loaded just to the left of J3 and are labelled POD1, POD2, and POD3.

The 25-pin strips, item 2, are loaded near J1 and J2. Traces on the printed circuit board connect the pins of J1 aand J2 to adjacent wiring pins.

Connectors. There are two types of connectors provided. At the J3 and J4 locations on the board, the 60-pin connectors (item 5 in table F-2) are installed on the top side of the board. See figure F-1 for placement. When placing these connectors on the board be sure that the pin 1 end (indicated by the triangle molded into the connector body) is at the bottom of the board where there is a "1" etched into the board.

Connectors that bring signals from the target system to the interface module at either the J1 or J2 location, or both, are supplied. These two connectors are both 40-pin connectors; item 1 in table F-2. These two connectors can be oriented in either direction to accommodate the cables from the target system.

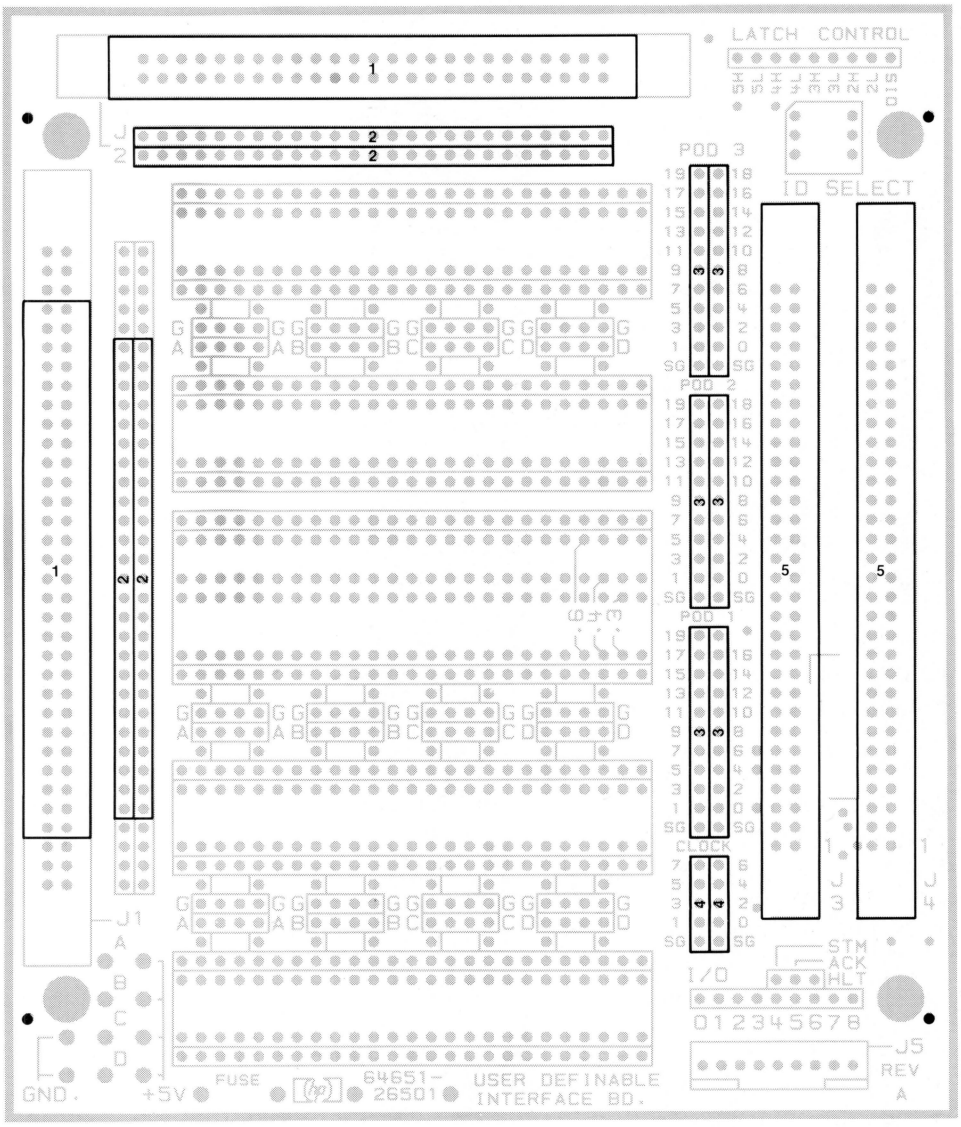

Figure F-1. Wire Wrapping Interface Module Component Loading Diagram

Hardware. The mechanical hardware supplied includes the screws, spacers, sheet metal panel and cable strain relief bracket needed to complete the assembly of the interface module. The description of these parts and how they are assembled in the final assembly process is discussed later in this appendix.

Components Supplied with the Microprocessor Interface Kit

Components required by the interface module design for support of active circuitry (excluding the active circuitry itself) are provided in the Microprocessor Interface Kit. These parts include sockets, bypass capacitors, an identification code select switch, and power fuses. These are discussed in the following paragraphs. Figure F-2 shows a view of the component parts that are supplied with the kit. Item numbers are included that reference table F-3.

Table F-3. Microprocessor Interface Kit Components

Item #	Description	HP Part #	Quantity
1	CONN-POST TYPE 9-PIN	1251-7613	1
2	SOCKET-IC 14 PIN DIP	1200-0638	5
3	SOCKET-IC 16 PIN DIP	1200-0607	5
4	SOCKET-IC 20 PIN DIP	1200-0639	5
5	SOCKET-IC 24 PIN DIP	1200-0541	2
6	CAP-FXD .1uf +80-20%	0160-5246	24
7	PCB SWITCH - 16 POS	3100-1675	1
8	FUSE 1A 125V	2110-0099	2
9	CONN-POST TYPE 3-PIN	1251-4682	1
10	CONN-POST TYPE 4-PIN	1251-5394	24
11	CONN-POST TYPE 9-PIN	1251-7697	4
12	CONN-POST TYPE 25-PIN	1251-4773	10

Component Sockets. There are five rows of pads on the printed circuit board where sockets for dual in-line style components may be loaded. These sockets are items 2, 3, 4, and 5 in table F-3. According to figure F-2, one each of items 2, 3, and 4 are loaded into each of the five rows. Using this approach, a single, long socket with 25 pins on each side will result and all five of each items 2, 3, and 4 will be used. Integrated circuits may be placed anywhere along this socket strip. Alternately, any of the item 2, 3, or 4 sockets may be placed anywhere along the five rows. This way there will be an individual socket for each integrated circuit. Either approach is acceptable; the decision is completely up to the user.

One additional area of flexibility is found on the middle row of sockets. This row will accommodate sockets with spacing between the leads of 0.3, 0.4, or 0.6 inches. The other four rows will only accept sockets with spacing of 0.3 inch. Toward the right end of the middle row are the numbers ".3", ".4", and ".6" with some lines that point to the two rows of holes that should be used for sockets with that lead spacing. Two 24-pin sockets, item 5 in table F-3, may be loaded in the third row instead of the item 2, 3, or 4 sockets. They may be placed next to each other if a 40-or 48-pin socket is needed or separated by one hole position if two 24-pin sockets are needed.

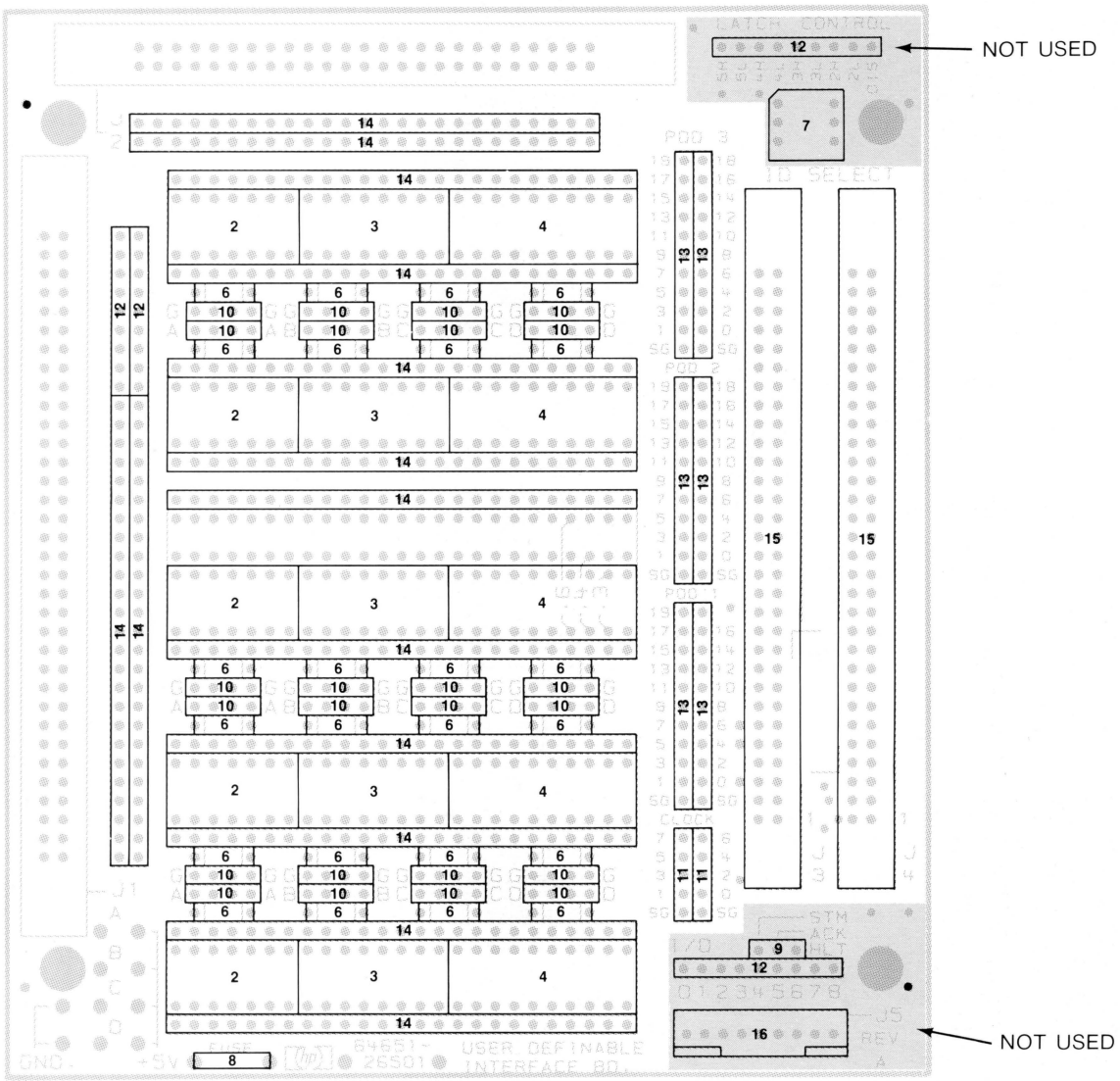

Figure F-2. Microprocessor Interface Kit Component Loading Diagram

Wiring Pins. The Microprocessor Interface Kit includes additional wiring pins similar to those in the Wire Wrapping Interface Module. These are discussed below.

The 3-pin strip, item #9, is installed in the lower right corner of the interface board. It provides access to the $\overline{\text{STM}}$ (STIMULUS), $\overline{\text{ACK}}$ (ACKNOWLEDGE), and $\overline{\text{HLT}}$ (HALT) lines.

The 4-pin strips, item 10, connect to the power ground plane and to the four power buses A, B, C, and D. There are 24 of these pins that are loaded through the middle section of the board. There will be a letter (A, B, C, D, or G) on either end of each of the 4-pin strips.

The 9-pin strips, item 11, are loaded in several places on the board. One strip is loaded at the upper right corner of the board and is labelled "LATCH CONTROL". The second strip is loaded at the lower right corner just below the three-pin strip. These pins give access to the nine INPUT/OUTPUT wires on the preprocessor endcap. The last two 9-pin strips are used along with two 25-pin strips just to the right of the the J1 connector area if a connector larger than 50 pins is used at the J1 location.

The 25-pin strips, item 12, are also loaded at several places on the board. One strip is placed on either side of the five rows of component sockets. Etched traces on the printed circuit board connect these wiring pins to the adjacent pins of the component sockets. The remaining item 12 pin strips are loaded next to J1 and J2; traces on the printed circuit board connect J1 and J2 to their respective wiring pins.

Bypass Capacitors. Provision has been made on the interface board for power supply distribution and capacitive bypassing. There are four power buses on the board; they are labeled A, B, C, and D. For each power bus space is provided for six 0.1uf capacitors near the wiring pins. Item 6 in table F-3 is the capacitor; figure F-2 shows the 24 capacitors generally spread out through the middle of the board.

Power Fuse. A 1-amp fuse is supplied to protect the general purpose probe interface and logic analyzer when +5V power is obtained from the logic analyzer. Two fuses are provided; one is a spare. The fuses are item 8 in table F-3

If you are going to use the +5V power from the logic analyzer, install the fuse at the lower left corner of the interface board in the two holes just below the label "FUSE" (see figure F-2). The fuse may be soldered directly on the board or it can be mounted on terminal pins that are first soldered to the board. You must supply the terminal pins for this use.

CAUTION

If +5V power is supplied by the probe interface, the 1-amp fuse must be used to protect the probe interface and logic analyzer from damage.

User Supplied Components

Any components required by the interface module design but not discussed in the previous section must be identified and supplied by the user. Examples of such components would include any integrated circuits or discrete circuit components, wire wrap wire and tools, and any connectors or cables required to connect to the target system. The user should identify any component requirements as early as possible in the project so that they may be ordered in time to be on hand when needed.

Power Supply Distribution

The printed circuit board can distribute from one to four power supply voltages to components on the board. The four power buses are labeled "A", "B", "C", and "D". At the lower left corner of the interface board, there are four holes also labeled "A" thru "D" (see figure F-2). These holes are used to connect voltage sources to the four power buses. The four buses, power ground, and signal ground are described in the following paragraphs. See figure F-3.

Using +5V from the 1630A/D

The circuitry on the interface module can receive +5 volts at up to 1 amp from the logic analyzer through the general purpose probe interface. To connect the A, B, C, or D power bus to the logic analyzer +5-volt supply, install a jumper wire from the hole with the same letter to the adjacent hole labeled "+5v". A jumper wire must be installed for each bus to be connected to +5 volts.

User Supplied Power

If +5 volts is not appropriate power for circuitry on the interface board, the four power buses can be connected to supplies in the target system. By connecting the four holes labeled A thru D to wires from the target system, any voltages can be supplied. Two other holes labeled "GND" are provided for the ground return of the target system power supply. A combination of target system supplied and analyzer supplied power can be used as long as different power buses (A thru D) are used. Ensure that power supply voltages from the target system are never connected to the +5-volt supply from the logic analyzer. Be sure to fuse power supplies from the target system.

Bypass Capacitors

There are 24 0.1-uF ceramic capacitors provided for bypassing the power supplies of any active circuitry on the interface board. For each power bus, install up to six bypass capacitors near the wiring pins.

Power Ground Connections

The 4-pin strips with "G" at each end are connected to the power ground plane of the printed circuit board. This ground plane is also the +5V power supply ground of the probe interface and logic analyzer. Make ground connections for any circutry on the interface board to the wiring pins labeled "G". One hole for each bypass capacitor on the interface board is also connected to this power ground plane.

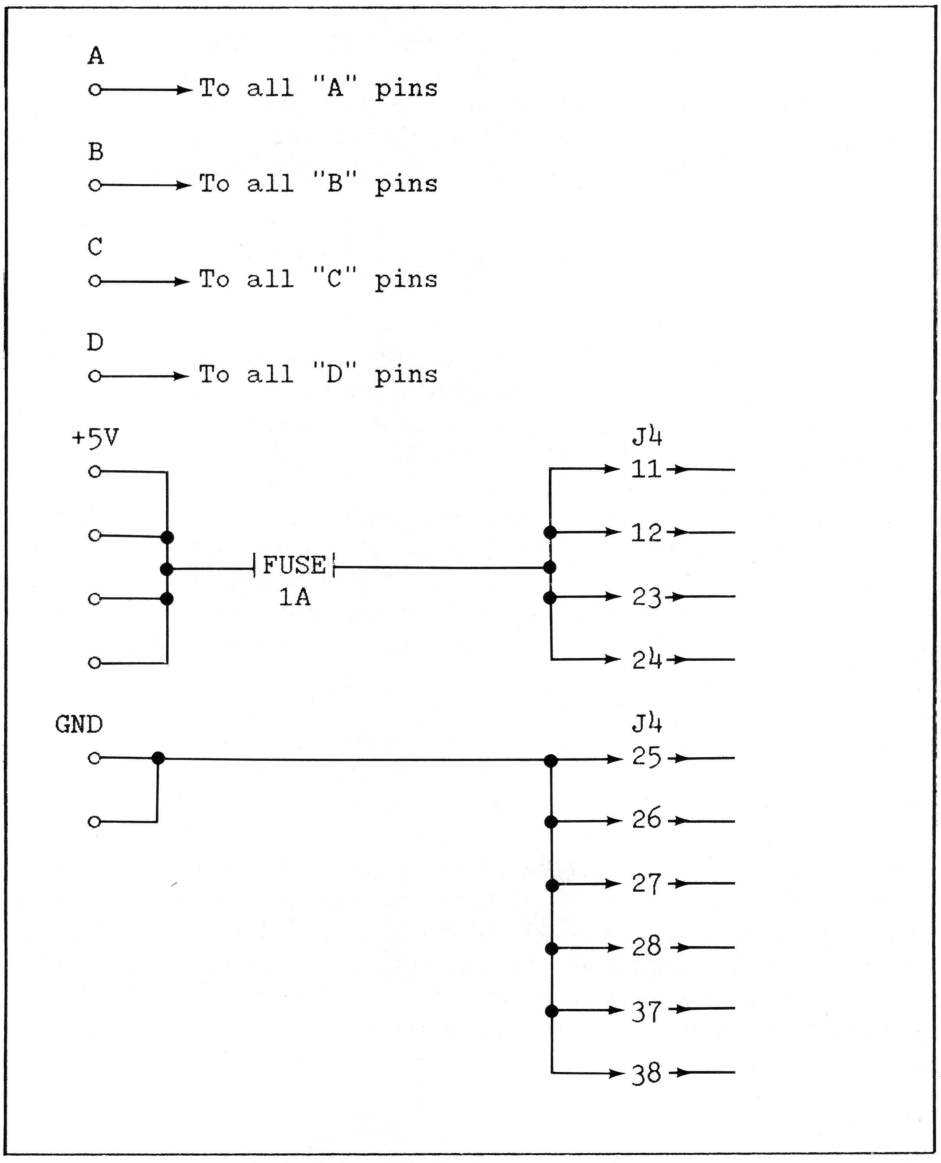

Figure F-3. Power Distribution Wiring Diagram

Signal Ground Connections

The logic analyzer can vary its data and clock thresholds from +10 volts to -10 volts. The signal ground reference for this control is available on the interface module printed circuit board. There is a separate ground reference for the clock channels and for each 20 data channels. These grounds are available on the wiring pins labeled "SG" that are grouped with each set of wiring pins. If no active circuitry is on the interface board, connect the signal grounds to the ground reference at the target system (not the interface board power ground). Route the signal ground to the target system over the same cables that carry the clock and data signals. If circuitry on the interface board is driving the logic analyzer inputs, connect the signal grounds of that circuitry to the power ground pins labeled "G".

If the signals of the target system all operate using the same threshold, jumper the signal grounds together. If the signals of the target system operate on different thresholds (TTL for some and ECL for others, for example), be sure that the signal and ground connections for each threshold are routed through the same 20-pin pod wiring pins.

Wiring the Interface Module

With the exception of the printed wiring traces, all interconnections between components on the board must be done using wirewrap techniques. Arrange the component layout with wire length and routing in mind. Keep all interconnections as short as possible.

Make all of your wire wraps on the component side of the board. This allows the board to be mounted on the sheet metal cover provided. Then the completed assembly can be installed in the general purpose probe interface. Route the wires down rows between components instead of over components. This allows installation and replacement of components after the wiring is completed.

To Target System Connectors

Mount connectors from the target system in the sets of holes labeled "J1" and "J2" (see figure F-2). Next to the J1 and J2 areas are dual rows of wiring pins. Etched traces on one of the inner layers of the printed circuit board connect the holes of J1 and J2 to corresponding wiring pins. Use these wiring pins to make connections from the target system to other parts of the interface board.

Between Components on the Interface Module

Make connections between components on the interface board, if any, using wirewrap techniques. Each pin of the component sockets is connected through an inner layer etched trace to an adjacent wiring pin. Use these pins to make connections to other components on the board or to connectors that carry signals off the board.

To General Purpose Probe Interface Connectors

All signal connections to buckets A through E on the general purpose probe interface have also been brought out to wiring pins. The module is designed for use in other probe interfaces which have three 20-pin pods (called POD1, POD2, and POD3) and an 8-channel clock pod (CLOCK). The user definable printed circuit board is labeled for these connections. Table F-4 shows the interconnections from pins in the POD and CLOCK groups to the interface module buckets labeled A, B, C, D, and E.

Table F-4. Interface Signal Interconnections

Logic Analyzer Probe:Bit	10269A Bucket:Bit	Cable Conn:Bit	Interface Board Pod:Bit
0:0	A:0	J3:45	2:4
0:1	A:1	J3:46	2:5
0:2	A:2	J3:47	2:6
0:3	A:3	J3:48	2:7
0:4	A:4	J3:49	2:8
0:5	A:5	J3:50	2:9
0:6	A:6	J3:51	2:10
0:7	A:7	J3:52	2:11
Not Used	A:8	J3:41	2:0
Ground	A:9	J3:38	2:SG
Not Used	A:10	J3:19	CLOCK:3
1:0	B:0	J3:53	2:12
1:1	B:1	J3:54	2:13
1:2	B:2	J3:55	2:14
1:3	B:3	J3:56	2:15
1:4	B:4	J3:57	2:16
1:5	B:5	J3:58	2:17
1:6	B:6	J3:59	2:18
1:7	B:7	J3:60	2:19

Table F-4. Interface Signal Interconnections (Cont'd)

Logic Analyzer Probe:Bit	10269A Bucket:Bit	Cable Conn:Bit	Interface Board Pod:Bit
Not Used	B:8	J3:42	2:1
Ground	B:9	J3:13	CLOCK:SG
Not Used	B:10	J3:23	CLOCK:0
2:0	C:0	J4:1	1:0
2:1	C:1	J4:2	1:1
2:2	C:2	J4:3	1:2
2:3	C:3	J4:4	1:3
2:4	C:4	J4:5	1:4
2:5	C:5	J4:6	1:5
2:6	C:6	J4:7	1:6
2:7	C:7	J4:8	1:7
2:8	C:8	J4:9	1:8
Ground	C:9	J4:29	1:SG
L Clock	C:10	J3:17	CLOCK:2
3:0	D:0	J4:10	1:9
3:1	D:1	J4:13	1:10
3:2	D:2	J4:14	1:11
3:3	D:3	J4:15	1:12
3:4	D:4	J4:16	1:13
3:5	D:5	J4:17	1:14
3:6	D:6	J4:18	1:15
3:7	D:7	J4:19	1:16
3:8	D:8	J4:20	1:17
Ground	D:9	J4:31	1:SG
K Clock	D:10	J3:21	CLOCK:1
4:0	E:0	J4:21	1:18
4:1	E:1	J4:22	1:19
4:2	E:2	J4:39	3:0
4:3	E:3	J4:40	3:1
4:4	E:4	J4:42	3:3
4:5	E:5	J4:43	3:4
4:6	E:6	J4:44	3:5
4:7	E:7	J4:45	3:6
4:8	E:8	J4:46	3:7
Ground	E:9	J4:34	3:SG
J Clock	E:10	J3:23	CLOCK:0

Final Assembly

After the interface module printed circuit board has been fully loaded, wired, and soldered it is ready for final assembly. This consists primarily of mounting the printed circuit board to its sheet metal cover and connecting the target system cables. Before this is done however, there are two things which should be checked. One is to verify that there are no cold or broken solder joints. The second is to either visually or electrically verify that there are no unwanted shorts on the back side of the board. A short could be caused by a solder bridge or a component lead bent over against another lead.

Hardware

The mechanical hardware supplied with the Wire Wrapping Interface Module includes the screws, spacers, sheet metal panel, and cable strain relief bracket needed to complete the assembly of the interface module. Table F-5 lists the descriptions and the HP part numbers for these components. The description of how to use these parts in the final assembly is discussed in this paragraphs that follow.

Table F-5. Hardware Provided

Description	HP Part Number	Quantity
Spacer 4-40 .125	0380-0843	4
Screw 4-40 .312	2200-0512	4
Screw 4-40 .250	0642-0081	2
Cover Assembly	64651-64102	1
Strain Relief Bracket	64651-01201	1

Spacers and Sheet Metal

Mount the four 4-40 threaded spacers to the back side of the printed circuit board, one at each corner. Either press these spacers into the board (if the proper press is available) or solder them to the board. Then attach the printed circuit board to the sheet metal cover using four screws and the threaded spacers provided. Locate the printed circuit board assembly so that the J1 area of the board is next to the side of the sheet metal cover that has the protective rubber edge. Figure F-4 shows an exploded view of the final assembly of the interface module.

Target System Cables and Strain Relief Bracket

Unless you use the optional probe cables described at the end of this appendix, you must supply the cables that connect the interface module to the target system. Select cables that are long enough to allow placing the probe interface in a suitable location relative to the target

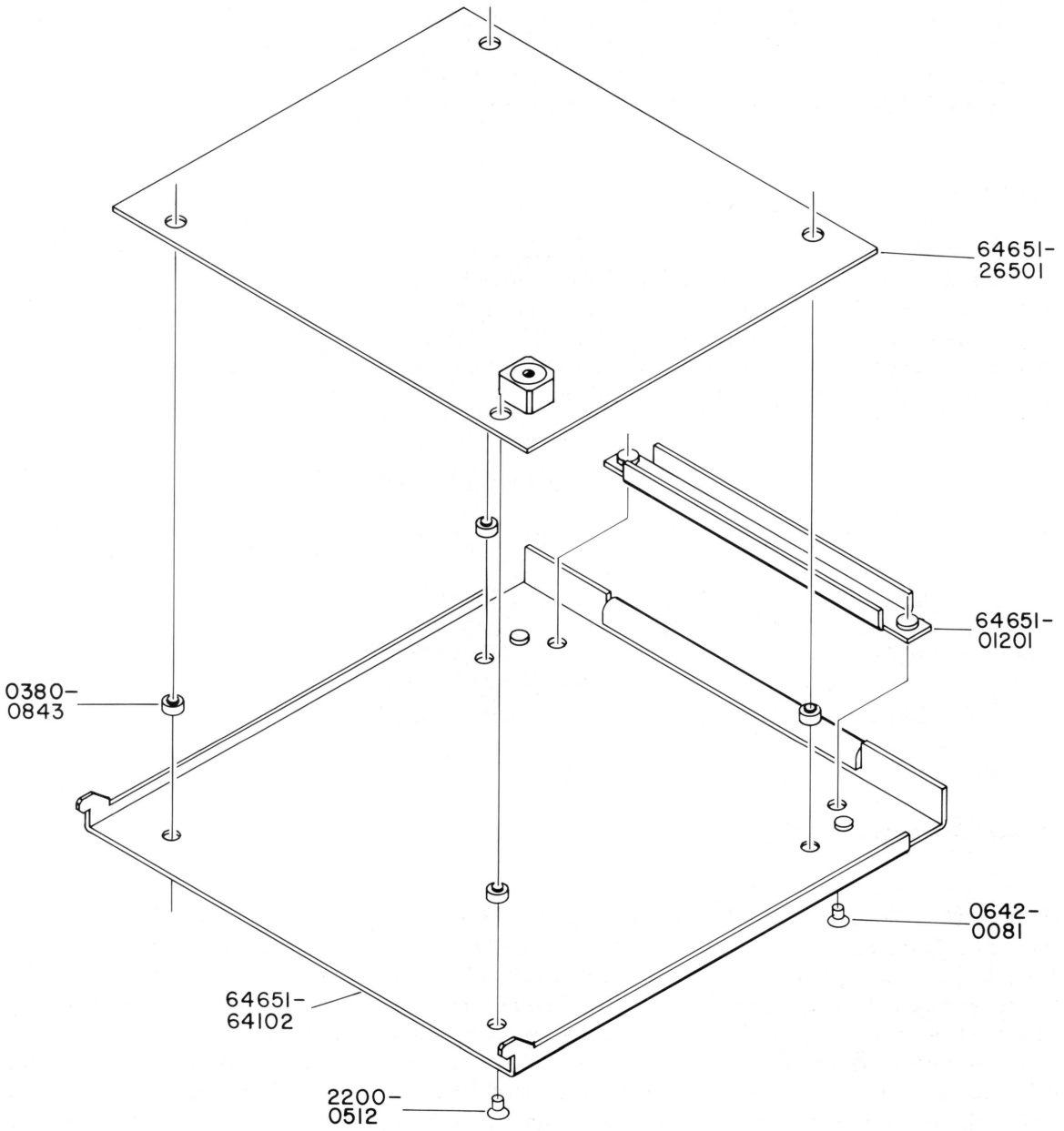

Figure F-4. Wire Wrapping Interface Module Exploded View

By alternating signals with ground wires in the cables, you can reduce crosstalk in long cables. When connecting the cables to the interface module, be sure pin 1 of the cable is connected to pin 1 of the connector. The cable from J1 can exit the interface module straight to the left and over the rubber protected edge of the sheet metal cover. If a cable is also connected to J2, a 90-degree fold must be made in the cable to allow it to exit to the left. Figure F-5 illustrates proper cable routing. Next, install the strain relief bracket over the target system cables and secure it with the two screws provided. See figure F-4 for the assembly diagram. When tightening the strain relief bracket, be sure that the cables do not pull the connectors.

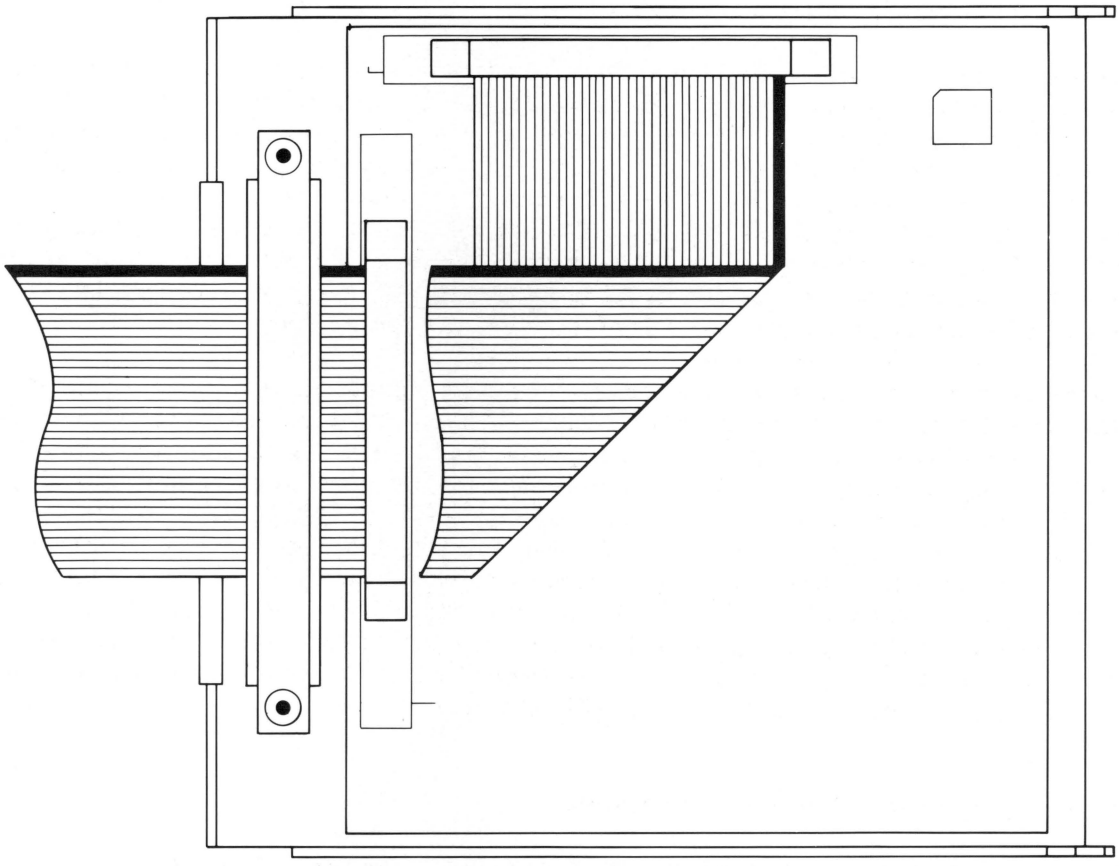

Figure F-5. Target Cable Installation

Initial Power Up

The following paragraphs provide guidelines for the first power up of the system and instructions on how to test the interface module. You can test the basic operation of the interface module along with the setup and hold of data relative to the analysis clock.

Checking Signal and Power Wiring Connections

Before applying power to the interface module, check all signal and power connections. Use continuity checks to verify that the power supply buses are connected to all of the appropriate component pins and that power supplies are not shorted to each other or to ground. If the target system supplies any power to the interface module, these supplies must be isolated from the +5-volt supply of the logic analyzer. Be sure all signal connections are made and no signals are incorrectly tied together.

Connection to the Target System and Preprocessor

After wiring connections have been checked, connect the interface module to the target system and probe interface. First, turn off power to the target system and the logic analyzer. If one of the optional probe cables is used for connection to the target system, remove the microprocessor or other device from its socket. Connect the probe cable into the socket and place the target device in the ZIF socket of the probe cable. Be sure that pin 1 of the target system socket, the probe cable, and the target device are all lined up. Any other type of probe cable should be appropriately connected to the target system.

Connect the interface module to the probe interface by first connecting the two 60-conductor flat cables to the J3 and J4 connectors of the interface module. Verify that the probe interface is properly connected to the logic analyzer. Apply power to the target system and the logic analyzer. Be sure the interface module does not interfere with operation of the target system. If the target system does not operate, verify that all connectors are properly installed and fully seated. If the target system still does not operate, there may be a wiring error or the design of the interface module may not be compatible with the target system. Measure power supply voltages on the interface module and verify that they are within specifications.

Verifying Operation of the Interface Module

Configure the logic analyzer for the target system. The logic analyzer operating manual explains how to set up the format and trace specifications. Then run a trace to ensure that the logic analyzer is receiving the desired clock signals. If "WARNING Slow Clock" appears on the display, or the operation does not seem to be correct, there are several areas to check. First, check the threshold selection of the logic analyzer. Then check the clock definition in the Format specification.

Be sure you specified the correct clock edge. Check the signal grounds of the probe interface for proper reference. These grounds are brought out to wiring pins on the interface module and must be connected either to the power ground on the interface board or to the ground reference in the target system. Refer to the section on signal ground connections in this appendix for more information.

If the logic analyzer seems to be clocking at the appropriate time intervals, check the address, data, and status (or other) fields in the list display for correctness. If any of the information is not correct, check the input thresholds in the format specification. Also check the label assignments to see that they specify the correct pods and bits. If just one or two bits of information are not correct, there may be an open circuit or an improper connection in those channels. In the trace specification, define a trigger and run a trace. Make another measurement using storage qualification. If all of the information captured by the logic analyzer is correct, the interface module is ready to use.

Optional Probe Cables For Dip Packages

There are three optional probe cable assemblies available for connecting the interface board to a target system. These cables connect to standard dual, in-line packages. Figure F-6 is a typical cable assembly exploded view. The following five parts make up each cable assembly:

(1). ZIF (Zero Insertion Force) socket (item #1): allows easy installation of the monitored device.

(2). Probe Cable (item #2): teflon insulated with ground wires between signal wires, a printed circuit board termination with pins and sockets, and a connector on the opposite end.

(3). Plastic Pin Guard (item #3): protects pins of the cable assembly when the cable is not connected to the target system. It is designed to fit over most low-profile sockets on target system boards.

(4). Socket (item#4): plugs onto the probe cable to protect its pins and hold the pin guard in place.

(5). Header (not shown): connects the cable to the interface board.

Normally the cable assembly is used fully assembled. The ZIF socket can be removed if a lower profile assembly is required. In this case, the microprocessor is connected directly into the printed circuit board on the probe cable. The pin guard can also be removed if it interferes with components on the target system. In this case, be sure to connect the socket to the probe cable to protect its pins. Then only the pins of the socket may be damaged, and a second socket is provided.

The three optional probe cable assemblies are options 102, 103, and 104. These options are for 40-, 48-, and 64-pin packages, respectively. Cable diagrams for these options are shown in Figures F-7 through F-9. Cable interconnections are shown in Tables F-6 through F-8. A 24-or 28-pin device can be connected using the 40-pin cable assembly.

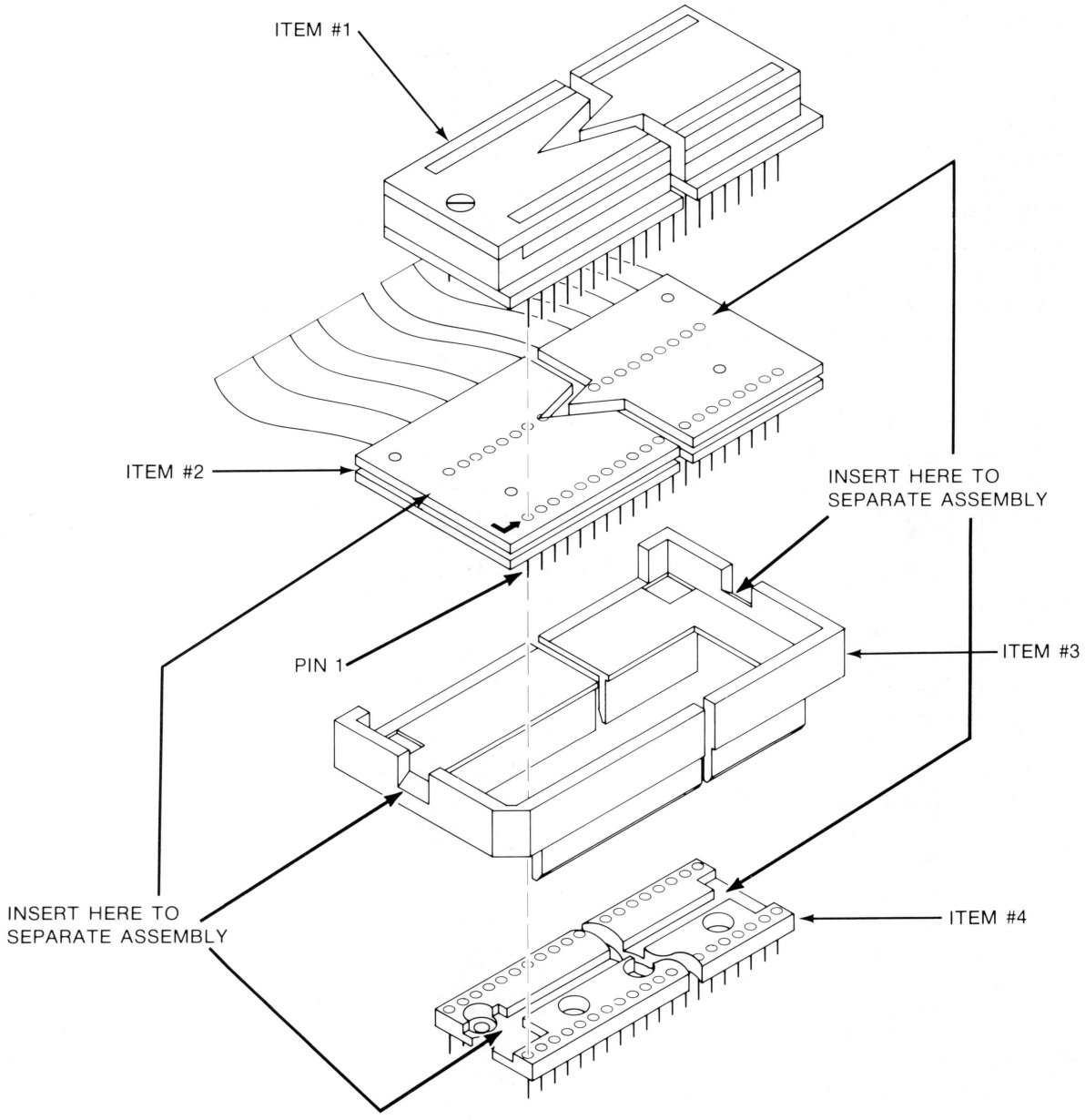

Figure F-6. Probe Cable Assembly Exploded View

Customizing the Cable for a Particular Device

Ground wires are placed between signal wires in the probe cable to reduce crosstalk between adjacent signals and enhance integrity of the data. At the target system end of the probe cable, all ground wires are terminated on a ground plane on top of the pin/socket board. Connect this ground plane to power supply ground in the target system by soldering a small wire from the top side of the pin/socket board to the ground plane. Be sure no signal pins are inadvertantly connected to the ground plane.

All pins of the target device are connected to signal wires in the cable. Some of these may not be needed in the interface module. Usually, the 20 to 25 pF cable capacitance will not affect these pins, but sometimes even this small capacitive load is not acceptable. One example is the crystal oscillator inputs of a microprocessor. These are so sensitive that the oscillator may not start with the additional capacitance. The solution is to cut the trace that connects the pin to the cable on the bottom side of the pin/socket board. Be careful not to damage any other traces or any of the pins on the circuit board. Cut only those traces to pins that cannot tolerate the cable capacitance. Keep all other pins, whether used or not.

Connecting Cable To The Interface

The connector at the interface module end of the probe cable is a socket for connecting onto a header or set of pins. This socket connector has more pins than the connector at the target system end of the cable. The additional pins connect to the ground wires between the signal wires in the cable. For example, the 40-pin probe cable has a 50-pin connector; 10 of the pins connect to ground wires. For each probe cable, this appendix shows a diagram of the numbering convention and a table that specifies pin connections.

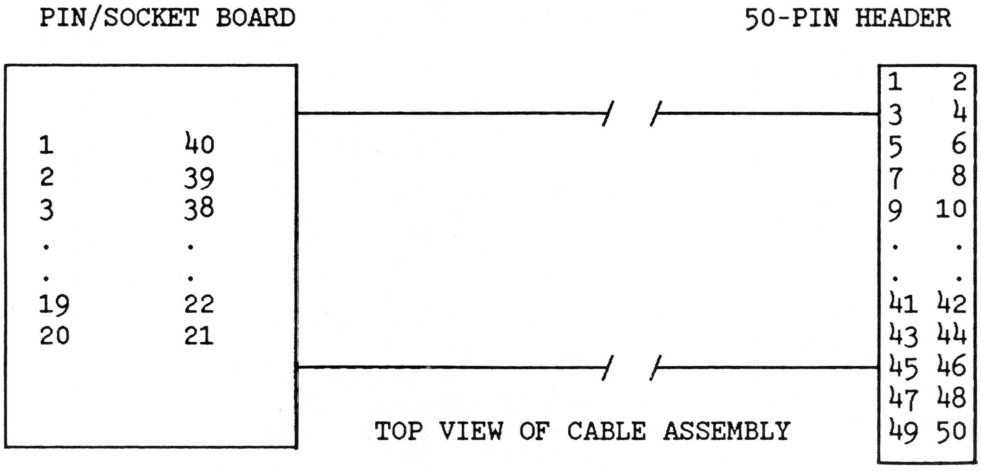

Figure F-7. Diagram of 40-Pin Probe Cable

Table F-6. 40-Pin Probe Cable Interconnections

50-PIN HEADER	PIN/SOCKET BOARD PIN #	50-PIN HEADER	PIN/SOCKET BOARD PIN #
1	GND	26	30
2	GND	27	12
3	GND	28	29
4	GND	29	13
5	1	30	28
6	40	31	14
7	2	32	27
8	39	33	15
9	3	34	26
10	38	35	24
11	4	36	25
12	37	37	17
13	5	38	24
14	36	39	18
15	6	40	23
16	35	41	19
17	7	42	22
18	34	43	20
19	8	44	21
20	33	45	GND
21	9	46	GND
22	32	47	GND
23	10	48	GND
24	31	49	GND
25	11	50	GND

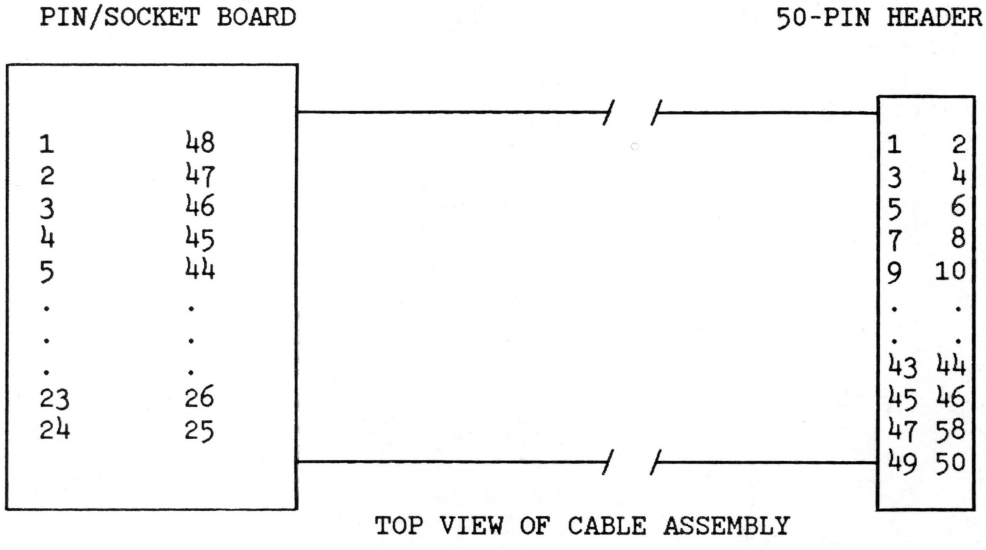

Figure F-8. Diagram of 48-Pin Probe Cable

Table F-7. 48-Pin Probe Cable Interconnections

50-PIN HEADER	PIN/SOCKET BOARD PIN #	50-PIN HEADER	PIN/SOCKET BOARD PIN #
1	1	26	36
2	48	27	14
3	2	28	35
4	47	29	15
5	3	30	34
6	46	31	16
7	4	32	33
8	45	33	17
9	5	34	32
10	44	35	18
11	6	36	31
12	43	37	19
13	7	38	30
14	42	39	20
15	8	40	29
16	41	41	21
17	9	42	28
18	40	43	22
19	10	44	27
20	39	45	23
21	11	46	26
22	38	47	24
23	12	48	25
24	37	49	GND
25	13	50	GND

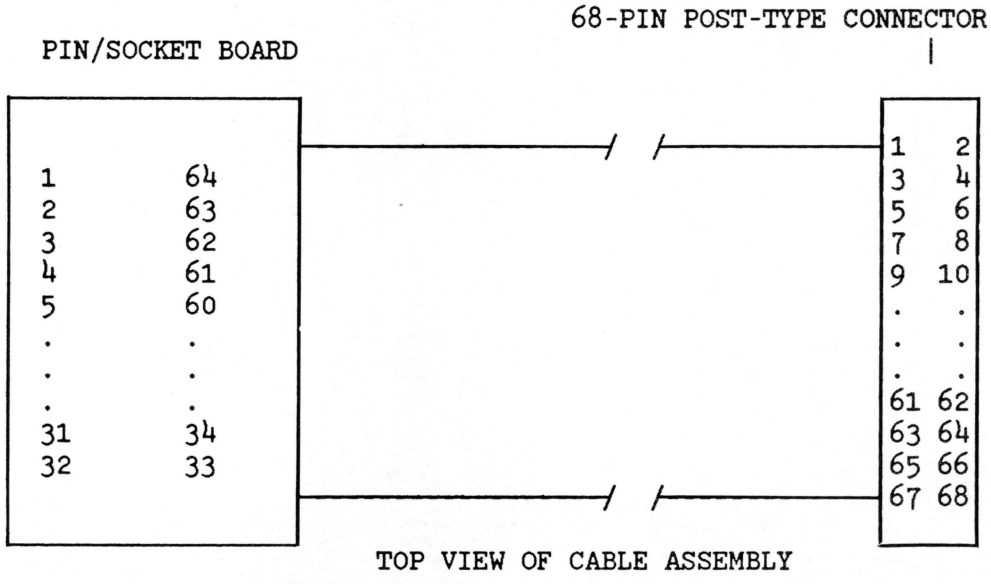

Figure F-9. Diagram of 64-Pin Probe Cable

Table F-8. 64-Pin Probe Cable Interconnections

68-PIN POST-TYPE	PIN/SOCKET BOARD PIN #	68-PIN POST-TYPE	PIN/SOCKET BOARD PIN #
1	GND	35	17
2	GND	36	48
3	1	37	18
4	64	38	47
5	2	39	19
6	63	40	46
7	3	41	20
8	62	42	45
9	4	43	21
10	61	44	44
11	5	45	22
12	60	46	43
13	6	47	23
14	59	48	42
15	7	49	24
16	58	50	41
17	8	51	25
18	57	52	40
19	9	53	26
20	56	54	39
21	10	55	27
22	55	56	38
23	11	57	28
24	54	58	37
25	12	59	29
26	53	60	36
27	13	61	30
28	52	62	35
29	14	63	31
30	51	64	34
31	15	65	32
32	50	66	33
33	16	67	GND
34	49	68	GND

Model 10269A Option Parts List and Wiring Diagram

This section contains information for ordering parts for the Model 10269A General Purpose Probe Interface options. Tables F-9 and F-10 list all replaceable parts for the Option 100 Wire Wrapping Interface Module and the Option 101 Microprocessor Interface Kit. Tables F-11 through F-13 list the replaceable parts for the 102, 103, and 104 Cable Assembly Options. Table F-14 contains the list of manufacturers' codes. To order a part listed in the tables, quote the Hewlett-Packard part number, indicate the quantity, and address the order to the nearest Hewlett-Packard office. In addition to the parts lists, this section contains a wiring diagram (see figure F-10) of the etched Printed Circuit Board, Part Number 64651-26501, which is part of the Wire Wrapping Interface Module.

Option 100--Wire Wrapping Interface Module

The parts list for the Option 100 Wire Wrapping Interface Module is given in table F-9.

Table F-9. Option 100--Wire Wrapping Interface Module Parts List

HP PART NUMBER	CD	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
1251-4773	6	4	CONN-POST TYPE 25-PIN	03418	22-10-2251
1251-5395	0	2	CONN-POST TYPE 5-PIN	03418	22-10-2051
1251-3004	4	2	CONN-HEADER 40-PIN	04726	3432-2002
1251-7575	2	2	CONN-HEADER 60-PIN	03206	65863-213
1251-7950	7	6	CONN-POST TYPE 11-PIN	03418	22-10-2111
64651-01201	2	1	STRAIN RELIEF BRACKET	28480	64651-01201
64651-26501	7	1	PC BD ETCHED	28480	64651-26501
64651-64102	4	1	COVER ASSEMBLY	28480	64651-64102

Option 101--Microprocessor Interface Kit

The parts list for the Option 101 Microprocessor Interface Kit is given in table F-10.

Table F-10. Option 101--Microprocessor Interface Kit Parts List

HP PART NUMBER	CD	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
0160-5246	6	24	CAP-FXD .1UF +80-20%	02010	MD015E104MAA
1200-0541	1	2	SOCKET-IC 24-PIN DIP	02414	DILB24P-108
1200-0607	0	5	SOCKET-IC 16-PIN DIP	02414	DILB16P-108
1200-0638	7	5	SOCKET-IC 14-PIN DIP	02414	DILB14P-108
1200-0639	8	5	SOCKET-IC 20-PIN DIP	02414	DILB20P-108
1251-4682	6	1	CONN-POST TYPE 3-PIN	03418	22-10-2031
1251-4773	6	10	CONN-POST TYPE 25-PIN	03418	22-10-2251
1251-5394	9	24	CONN-POST TYPE 4-PIN	03418	22-10-2041
1251-7613	9	1	CONN-POST TYPE 9-PIN	03418	22-11-1091
1251-7697	9	4	CONN-POST TYPE 9-PIN	03418	22-10-2091
2110-0099	4	2	FUSE 1A 125V .281X.093	04703	275001
3100-1675	4	1	PCB SWITCH-16 POS	05735	230057GB

Option 102--40 Pin Cable Assembly

The Option 102 Cable Assembly is HP Part Number 64651-61601. It consists of the parts listed in table F-11.

Table F-11. Option 102, 40-Pin Cable Assembly Parts List

HP PART NUMBER	CD	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
1200-0682	1	2	SOCKET-IC 40-PIN DIP	05518	540-AG63D
1251-3090	8	1	CONN-50 PIN HEADER	04726	3433-2002
5041-3163	5	1	PIN BASE-40 PIN	28480	5041-3163
64651-66504	4	1	ZIF SOCKET BOARD-40 PIN	28480	64651-66504
8120-4080	8	1	CABLE-40 PIN PROBE	28480	8120-4080

Option 103--48 Pin Cable Assembly

The Option 103 Cable Assembly is HP Part Number 64651-61602. It consists of the parts listed in table F-12.

Table F-12. Option 103, 48-Pin Cable Assembly Parts List

HP PART NUMBER	CD	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
1200-0943	7	2	SOCKET-IC 48 DIP	05518	248-AG1A
1251-3090	8	1	CONN-50 PIN HEADER	04726	3433-2002
5041-3164	6	1	PIN BASE-48 PIN	28480	5041-3164
64651-66505	5	1	ZIF SOCKET BD-48 PIN	28480	64651-66505
8120-4081	9	1	CABLE-48 PIN PROBE	28480	8120-4081

Option 104--64 Pin Cable Assembly

The Option 104 Cable Assembly is HP Part Number 64651-61603. It consists of the parts listed in table F-13.

Table F-13. Option 104, 64-Pin Cable Assembly Parts List

HP PART NUMBER	CD	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
1200-0944	8	2	SOCKET-IC 64 PIN DIP	05518	264-AG1A
1251-8065	7	1	CONN-POST TYPE 68 PIN	03206	65610-168
5041-3165	7	1	PIN BASE-64 PIN	28480	5041-3165
64651-66506	6	1	ZIF SOCKET BD-64 PIN	28480	64651-66506
8120-4082	0	1	CABLE-64 PIN PROBE	28480	8120-4082

Table F-14. Manufacturers' Code List

MFR NO.	MANUFACTURERS' NAME	ADDRESS	ZIP CODE
28480	HEWLETT-PACKARD CO	PALO ALTO, CA	94304
02010	AVX CERAMICS CORP	MYRTLE BEACH, CA	29577
02414	BURNDY CORP	NORWALK, CT	06852
03418	MOLEX PRODUCTS CO	DOWNERS GROVE, IL	60515
03206	BERG ELEK DIV DUPONT	NEW CUMBERLAND, PA	17070
05518	AUGAT INC	ATTLEBORO, PA	02703
04726	3M COMPANY	ST PAUL, MN	55101
04703	LITTLEFUSE	DES PLAINES, IL	60016
05735	EECO INC	SANTA ANA, CA	92701

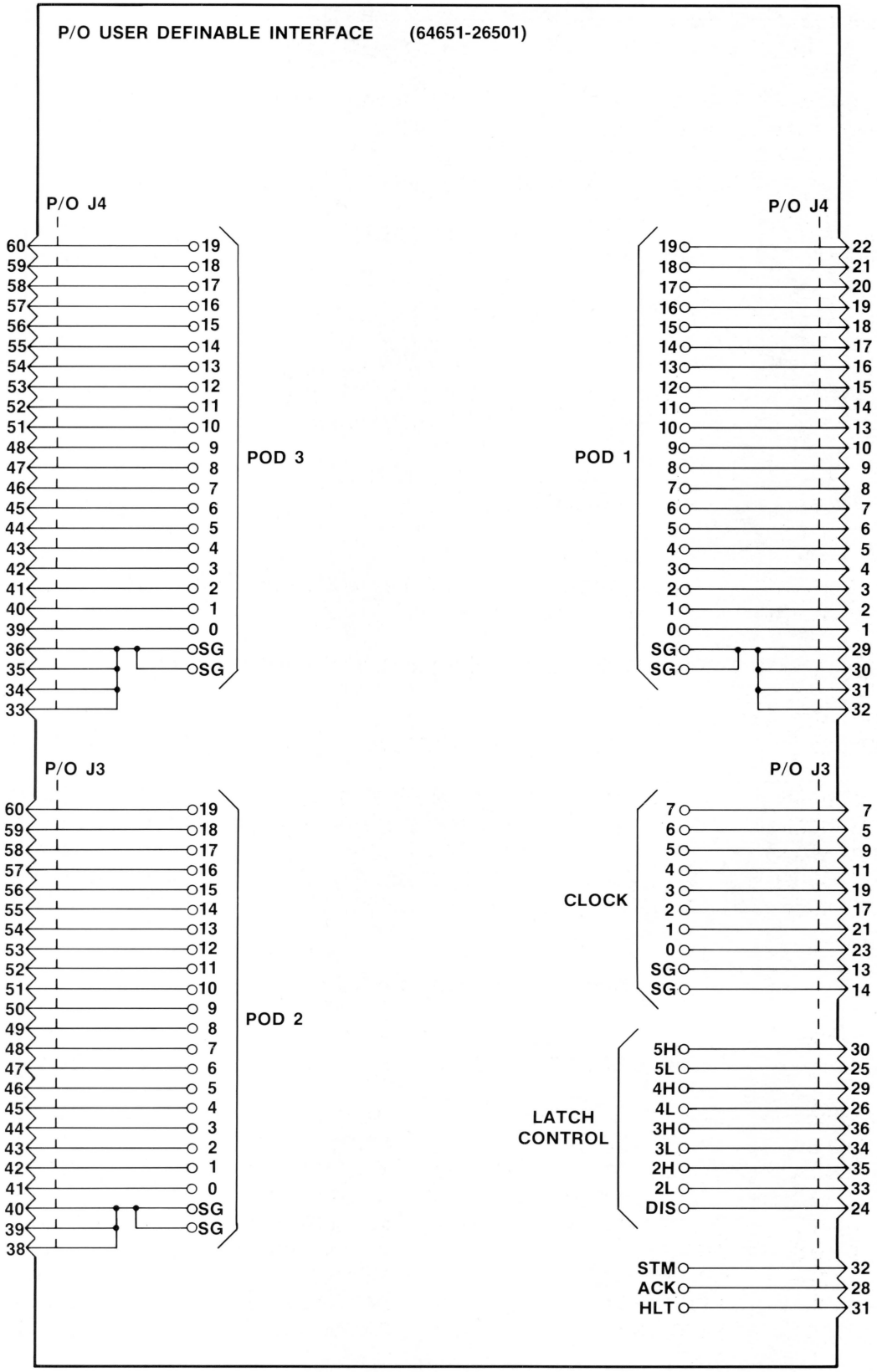

Figure F-10. Wire Wrapping Interface Module Wiring Diagram

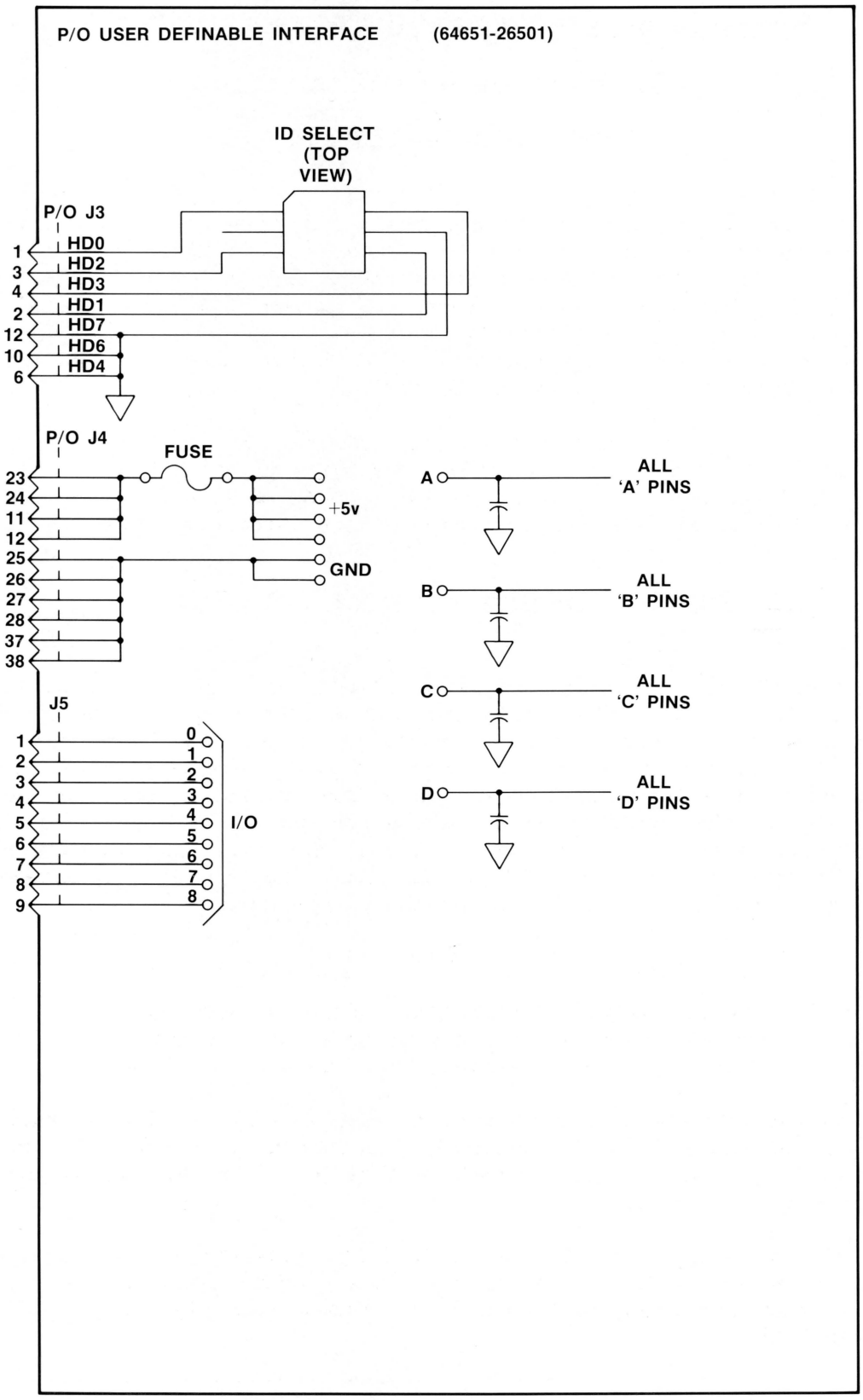

Figure F-10. Wire Wrapping Interface Module Wiring Diagram (Cont'd)

Interfacing to the PDP-11 Unibus® (10275A), LSI-11 Q-Bus® (10276A), and Intel Multibus® (52126A)

Hewlett-Packard provides interfaces that plug directly into mainframes for several popular minicomputer bus structures. These interfaces can supply signals to the 1630D when connected through the Model 10269A with the wire wrap board, Option 100, installed. The interfaces have all the signal conditioning and buffering required. The following pages show you how to wire wrap the signals from the interface board across the wire wrap board to the inputs of the 1630D.

Load the connectors and wire wrap pin strips onto the wire wrap board according to figure F-1. Then wire wrap the connections according to tables F-15 through F-17, as applicable. Connect J1 and J2 on the wire wrap board to JA and JB, respectively, on the interface board.

PDP-11 Unibus Interface (10275A)

The PDP-11 Unibus Interface monitors 18 address lines, 16 data lines, and 3 status lines. The following bus cycles can be qualified by switches on the interface board: processor or DMA, read or write, and interrupt acknowledge or normal. For example, processor writes can be qualified on the interface board. This qualification can also be accomplished in the 1630D trace specification when all three status signals are supplied. The DMA status line is not available on either the JA or JB connector of the 10275A. The DMA line can be supplied to an unused pin on connector JA by adding the wire described below.

NOTE

The following modification should be made by a Hewlett Packard service representative to ensure that the product warranty will remain in effect.

To bring the DMA status signal to connector JA, add a wire on the circuit side of the 10275-66502 Printed Circuit board. Connect it from U4 pin 9 to JA pin 4. The DMA signal will be high for DMA cycles and low for processor cycles.

After wire wrapping according to table F-15, interconnect the equipment and turn on the 1630D. Set up the [Assignment] menu of the Format Specification according to figure F-11. The status signals are defined in table F-18.

® PDP-11 Unibus and LSI-11 Q-Bus are Registered Trademarks of Digital Equipment Corporation.

® Multibus is a Registered Trademark of Intel Corporation.

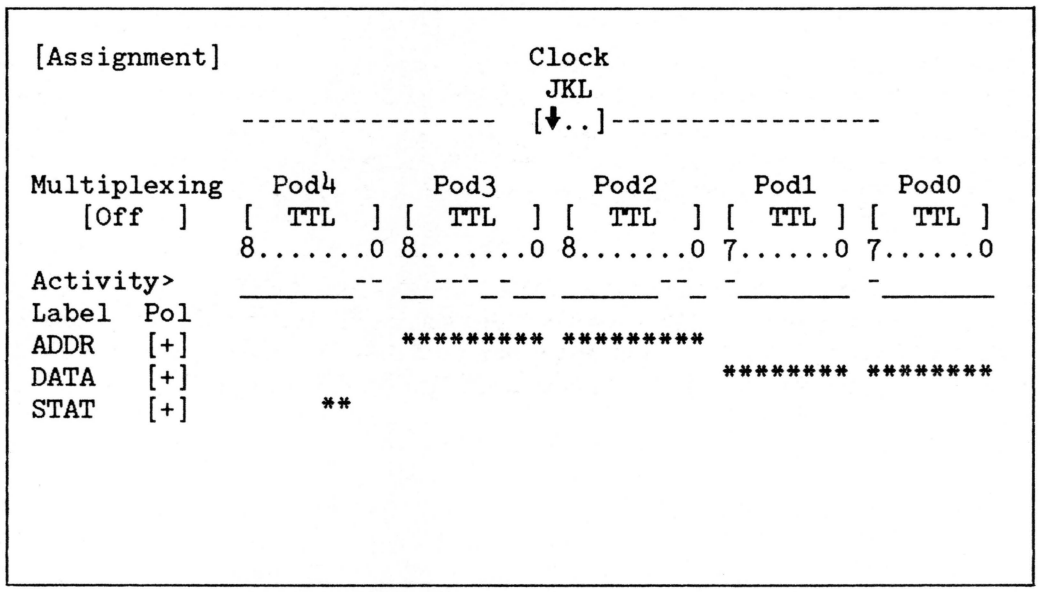

Figure F-11. PDP-11 Format Specification

LSI-11 Q-Bus Interface (10267A)

The LSI-11 Q-Bus Interface monitors 18 address lines, 16 data lines, and 5 status lines. The status lines indicate read or write, DMA, refresh, and interrupt acknowledge cycles.

After wire wrapping according to table F-16, interconnect the equipment and turn on the 1630D. Set up the [Assignment] menu of the Format Specification according to figure F-12. The status signals are defined in table F-18.

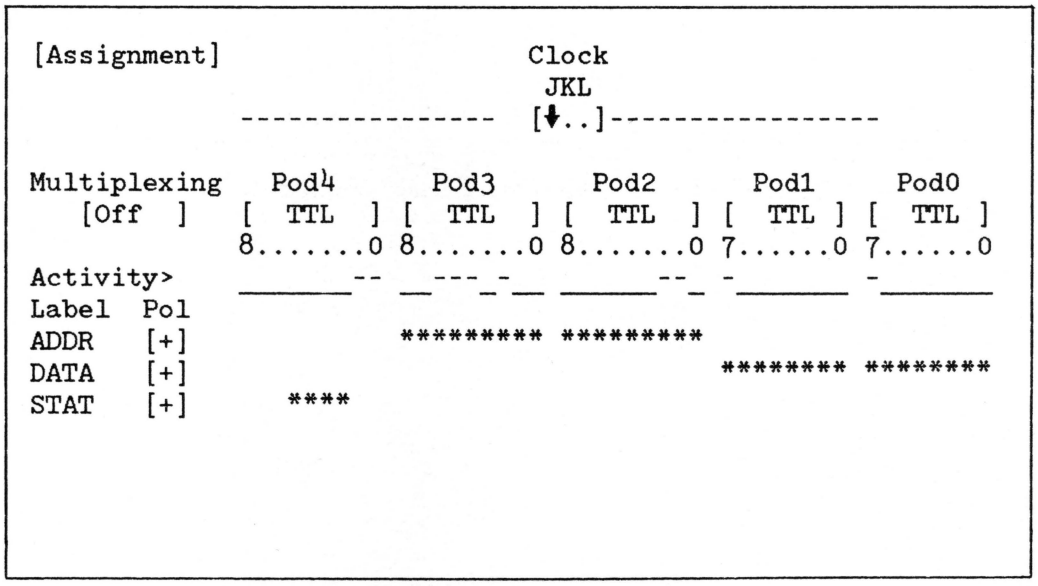

Figure F-12. LSI-11 Format Specification

Intel Multibus Interface (52126A)

The Intel Multibus Interface is designed to work with either an 8-bit or 16-bit data bus. Sixteen address lines are monitored. There are six active high status or command lines that indicate what type of transfer is being made on the bus. These status lines can be used for signal qualification in the analyzer, or for qualification by switches on the interface board.

After wire wrapping according to table F-17, interconnect the equipment and turn on the 1630D. (The 1630A can be used for monitoring an 8-bit data bus.) Set up the [Assignment] menu of the Format Specification according to figure F-13. The status signals are defined in table F-18.

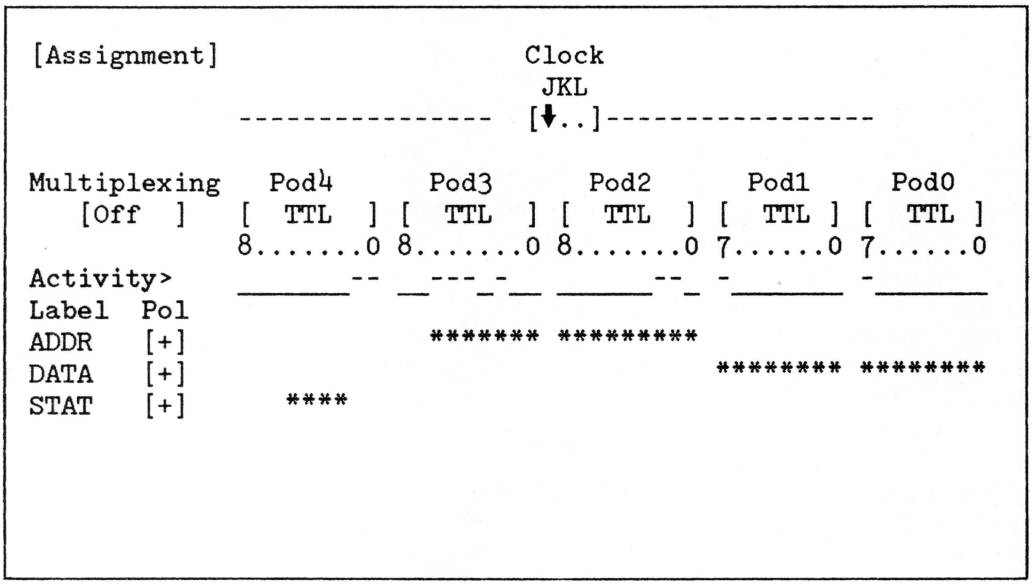

Figure F-13. Intel Multibus Format Specification

Table F-15. Connections For 1630D to PDP-11 Via Interface 10275A

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
D00	J2:37	2:4	A:0	0:0	DATA
D01	J2:35	2:5	A:1	0:1	DATA
D02	J2:33	2:6	A:2	0:2	DATA
D03	J2:31	2:7	A:3	0:3	DATA
D04	J2:29	2:8	A:4	0:4	DATA
D05	J2:27	2:9	A:5	0:5	DATA
D06	J2:25	2:10	A:6	0:6	DATA
D07	J2:23	2:11	A:7	0:7	DATA
		2:0	A:8	Not Used	
		2:SG	A:9	Ground	
		CLOCK:3	A:10	Not Used	
D08	J2:21	2:12	B:0	1:0	DATA
D09	J2:19	2:13	B:1	1:1	DATA
D10	J2:17	2:14	B:2	1:2	DATA
D11	J2:15	2:15	B:3	1:3	DATA
D12	J2:13	2:16	B:4	1:4	DATA
D13	J2:11	2:17	B:5	1:5	DATA
D14	J2:9	2:18	B:6	1:6	DATA
D15	J2:7	2:19	B:7	1:7	DATA
		2:1	B:8	Not Used	
		CLOCK:SG	B:9	Ground	
CLOCK	J2:5	CLOCK:0	B:10	Not Used	
A00	J2:40	1:0	C:0	2:0	ADDR
A01	J2:39	1:1	C:1	2:1	ADDR
A02	J2:38	1:2	C:2	2:2	ADDR
A03	J2:36	1:3	C:3	2:3	ADDR
A04	J2:34	1:4	C:4	2:4	ADDR
A05	J2:32	1:5	C:5	2:5	ADDR
A06	J2:30	1:6	C:6	2:6	ADDR
A07	J2:28	1:7	C:7	2:7	ADDR
A08	J2:26	1:8	C:8	2:8	ADDR
		1:SG	C:9	Ground	
		CLOCK:2	C:10	L Clock	
A09	J2:24	1:9	D:0	3:0	ADDR
A10	J2:22	1:10	D:1	3:1	ADDR
A11	J2:20	1:11	D:2	3:2	ADDR
A12	J2:18	1:12	D:3	3:3	ADDR
A13	J2:16	1:13	D:4	3:4	ADDR
A14	J2:14	1:14	D:5	3:5	ADDR
A15	J2:12	1:15	D:6	3:6	ADDR
A16	J1:17	1:16	D:7	3:7	ADDR
A17	J1:13	1:17	D:8	3:8	ADDR
		1:SG	D:9	Ground	
		CLOCK:1	D:10	K Clock	

Table F-15. Connections For 1630D to PDP-11 Via Interface 10275A (Cont'd)

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
		1:18	E:0	4:0	
		1:19	E:1	4:1	
READ(C1)	J1:33	3:0	E:2	4:2	STAT
INTR	J1:3	3:1	E:3	4:3	STAT
		3:3	E:4	4:4	
		3:4	E:5	4:5	
		3:5	E:6	4:6	
		3:6	E:7	4:7	
		3:7	E:8	4:8	
		3:SG	E:9	Ground	
CLOCK	J2:5	CLOCK:0	E:10	J Clock	

Notes: 1630D Probes plugged into 10269A in 16-bit order.
Connect wire wrap board J1 to JA on 10275A Interface.
Connect wire wrap board J2 to JB on 10275A Interface.

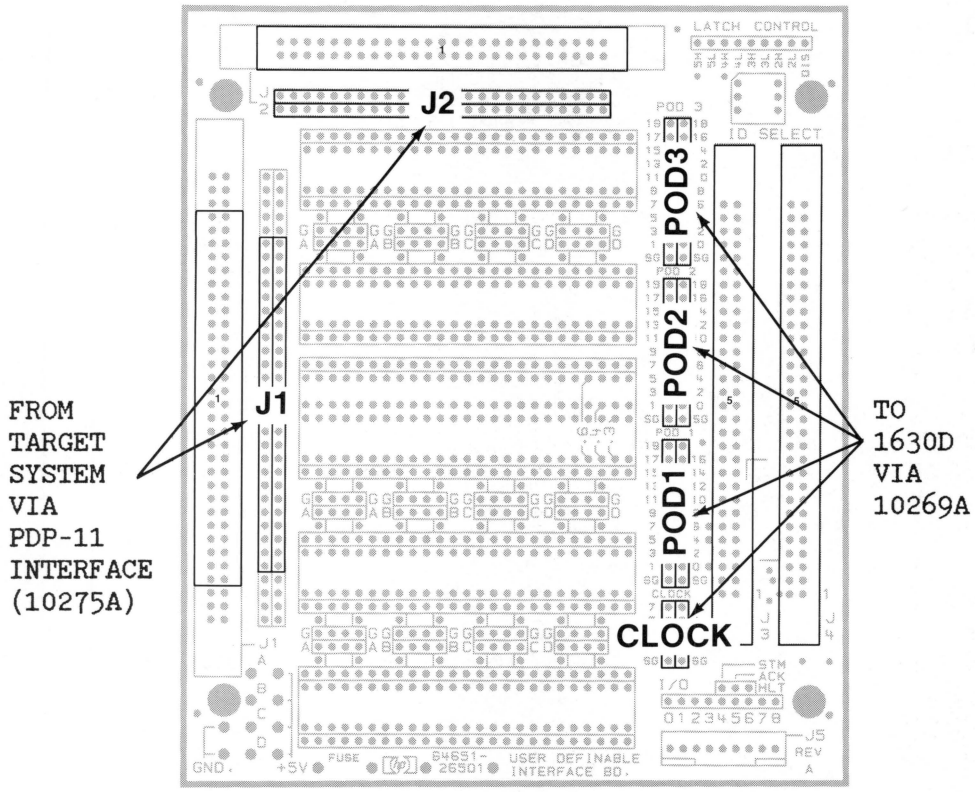

Figure F-14. Wire Wrap Board Wiring For 10275A

Table F-16. Connections For 1630D to LSI-11 Via Interface 10276A

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
D0	J2:37	2:4	A:0	0:0	DATA
D1	J2:35	2:5	A:1	0:1	DATA
D2	J2:33	2:6	A:2	0:2	DATA
D3	J2:31	2:7	A:3	0:3	DATA
D4	J2:29	2:8	A:4	0:4	DATA
D5	J2:27	2:9	A:5	0:5	DATA
D6	J2:25	2:10	A:6	0:6	DATA
D7	J2:23	2:11	A:7	0:7	DATA
		2:0	A:8	Not Used	
		2:SG	A:9	Ground	
		CLOCK:3	A:10	Not Used	
D8	J2:21	2:12	B:0	1:0	DATA
D9	J2:19	2:13	B:1	1:1	DATA
D10	J2:17	2:14	B:2	1:2	DATA
D11	J2:15	2:15	B:3	1:3	DATA
D12	J2:13	2:16	B:4	1:4	DATA
D13	J2:11	2:17	B:5	1:5	DATA
D14	J2:9	2:18	B:6	1:6	DATA
D15	J2:7	2:19	B:7	1:7	DATA
		2:1	B:8	Not Used	
		CLOCK:SG	B:9	Ground	
CLOCK	J2:5	CLOCK:0	B:10	Not Used	
A0	J2:40	1:0	C:0	2:0	ADDR
A1	J2:39	1:1	C:1	2:1	ADDR
A2	J2:38	1:2	C:2	2:2	ADDR
A3	J2:36	1:3	C:3	2:3	ADDR
A4	J2:34	1:4	C:4	2:4	ADDR
A5	J2:32	1:5	C:5	2:5	ADDR
A6	J2:30	1:6	C:6	2:6	ADDR
A7	J2:28	1:7	C:7	2:7	ADDR
A8	J2:26	1:8	C:8	2:8	ADDR
		1:SG	C:9	Ground	
		CLOCK:2	C:10	L Clock	
A9	J2:24	1:9	D:0	3:0	ADDR
A10	J2:22	1:10	D:1	3:1	ADDR
A11	J2:20	1:11	D:2	3:2	ADDR
A12	J2:18	1:12	D:3	3:3	ADDR
A13	J2:16	1:13	D:4	3:4	ADDR
A14	J2:14	1:14	D:5	3:5	ADDR
A15	J2:12	1:15	D:6	3:6	ADDR
A16	J1:17	1:16	D:7	3:7	ADDR
A17	J1:13	1:17	D:8	3:8	ADDR
		1:SG	D:9	Ground	
		CLOCK:1	D:10	K Clock	

Table F-16. Connections For 1630D to LSI-11 Via Interface 10276A (Cont'd)

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
		1:18	E:0	4:0	
		1:19	E:1	4:1	
RDIN	J1:33	3:0	E:2	4:2	STAT
RDOUT	J1:34	3:1	E:3	4:3	STAT
RSACK	J1:5	3:3	E:4	4:4	STAT
RREF	J1:22	3:4	E:5	4:5	STAT
		3:5	E:6	4:6	
		3:6	E:7	4:7	
		3:7	E:8	4:8	
		3:SG	E:9	Ground	
CLOCK	J2:5	CLOCK:0	E:10	J Clock	

Notes: 1630D Probes plugged into 10269A in 16-bit order.
Connect wire wrap board J1 to JA on 10276A Interface.
Connect wire wrap board J2 to JB on 10276A Interface.

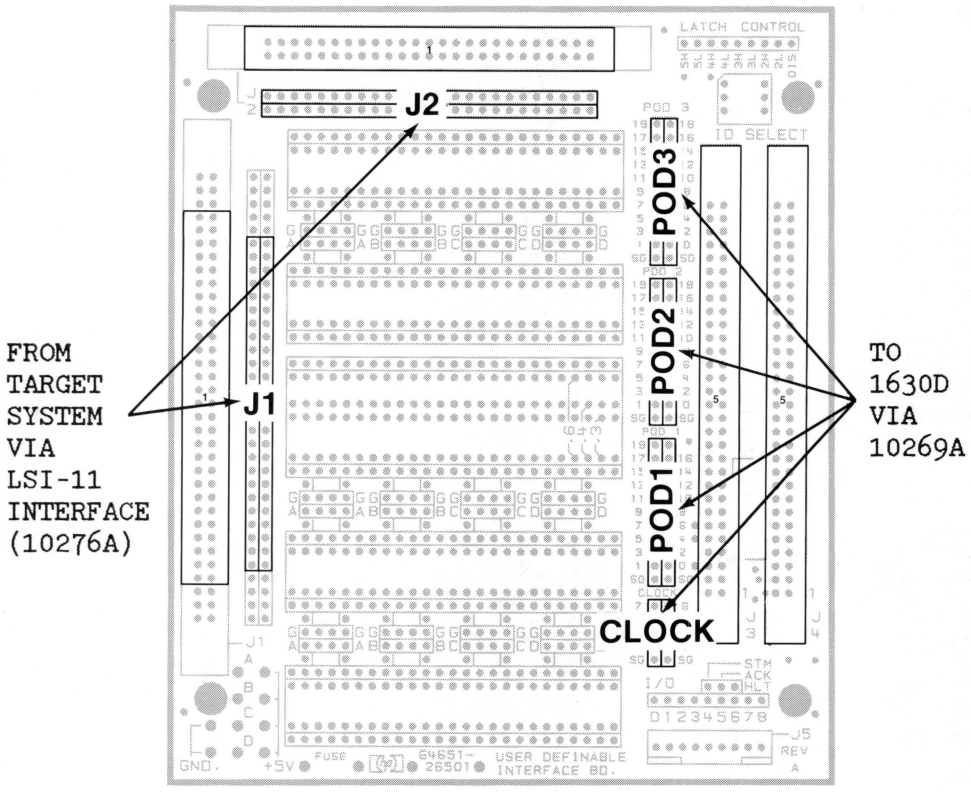

Figure F-15. Wire Wrap Board Wiring For 10276A

Table F-17. Connections For 1630D to Intel Multibus Via Interface 52126A

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
D0	J2:37	2:4	A:0	0:0	DATA
D1	J2:35	2:5	A:1	0:1	DATA
D2	J2:33	2:6	A:2	0:2	DATA
D3	J2:31	2:7	A:3	0:3	DATA
D4	J2:29	2:8	A:4	0:4	DATA
D5	J2:27	2:9	A:5	0:5	DATA
D6	J2:25	2:10	A:6	0:6	DATA
D7	J2:23	2:11	A:7	0:7	DATA
		2:0	A:8	Not Used	
		2:SG	A:9	Ground	
		CLOCK:3	A:10	Not Used	
D8	J2:21	2:12	B:0	1:0	DATA
D9	J2:19	2:13	B:1	1:1	DATA
D10	J2:17	2:14	B:2	1:2	DATA
D11	J2:15	2:15	B:3	1:3	DATA
D12	J2:13	2:16	B:4	1:4	DATA
D13	J2:11	2:17	B:5	1:5	DATA
D14	J2:9	2:18	B:6	1:6	DATA
D15	J2:7	2:19	B:7	1:7	DATA
		2:1	B:8	Not Used	
		CLOCK:SG	B:9	Ground	
CLOCK	J2:5	CLOCK:0	B:10	Not Used	
A0	J2:40	1:0	C:0	2:0	ADDR
A1	J2:39	1:1	C:1	2:1	ADDR
A2	J2:38	1:2	C:2	2:2	ADDR
A3	J2:36	1:3	C:3	2:3	ADDR
A4	J2:34	1:4	C:4	2:4	ADDR
A5	J2:32	1:5	C:5	2:5	ADDR
A6	J2:30	1:6	C:6	2:6	ADDR
A7	J2:28	1:7	C:7	2:7	ADDR
A8	J2:26	1:8	C:8	2:8	ADDR
		1:SG	C:9	Ground	
		CLOCK:2	C:10	L Clock	
A9	J2:24	1:9	D:0	3:0	ADDR
A10	J2:22	1:10	D:1	3:1	ADDR
A11	J2:20	1:11	D:2	3:2	ADDR
A12	J2:18	1:12	D:3	3:3	ADDR
A13	J2:16	1:13	D:4	3:4	ADDR
A14	J2:14	1:14	D:5	3:5	ADDR
A15	J2:12	1:15	D:6	3:6	ADDR
		1:16	D:7	3:7	
		1:17	D:8	3:8	
		1:SG	D:9	Ground	
		CLOCK:1	D:10	K Clock	

Table F-17. Connections For 1630D to Intel Multibus Via Interface 52126A (Cont'd)

Signal Name	Wire Wrap Board J1/J2	Wire Wrap Board POD:BIT	10269A Bucket:Bit	1630D Probe:Bit	Label
		1:18	E:0	4:0	
		1:19	E:1	4:1	
MWTC	J1:6	3:0	E:2	4:2	STAT
MRDC	J1:10	3:1	E:3	4:3	STAT
IOWC	J1:16	3:3	E:4	4:4	STAT
IORC	J1:15	3:4	E:5	4:5	STAT
		3:5	E:6	4:6	
		3:6	E:7	4:7	
		3:7	E:8	4:8	
		3:SG	E:9	Ground	
CLOCK	J2:5	CLOCK:0	E:10	J Clock	

Notes: 1630D Probes plugged into 10269A in 16-bit order.
Connect wire wrap board J1 to JA on 52126A Interface.
Connect wire wrap board J2 to JB on 52126A Interface.

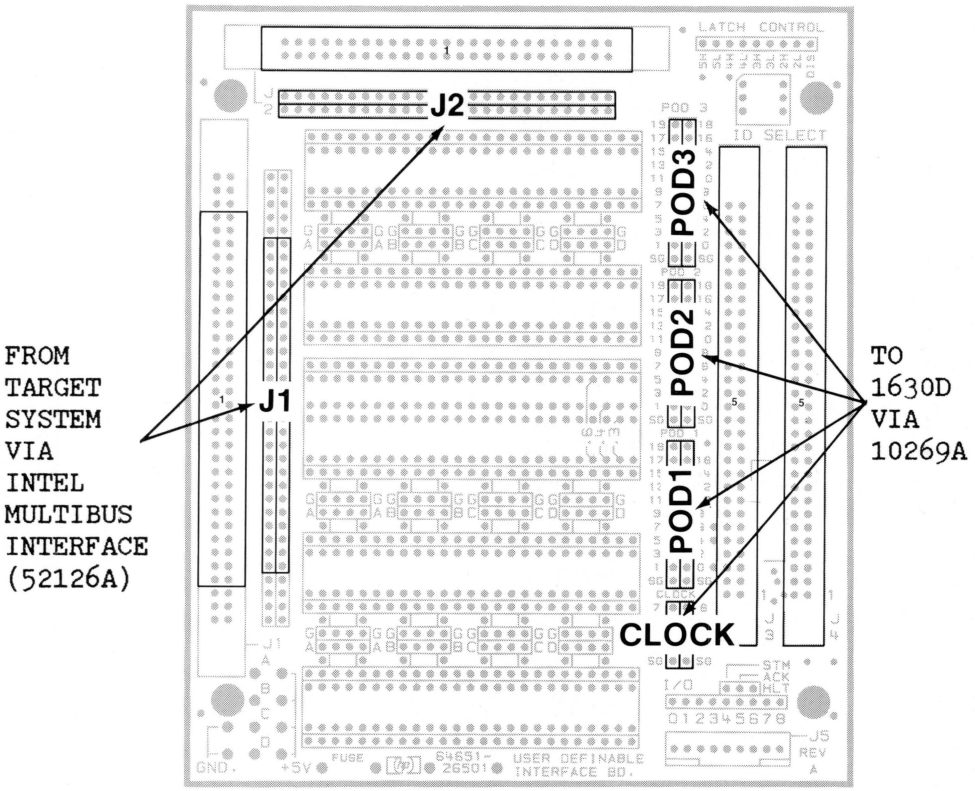

Figure F-16. Wire Wrap Board Wiring For 52126A

Table F-18. Status Line Mnemonics Definitions

PDP-11

READ(C1)	READ. This signal is high during read cycles and low during write cycles.
INTR	INTERRUPT. This signal is high when an interrupt vector number is on the bus, and low during other processor cycles.

LSI-11

RDIN	READ IN. This signal is high when the master is ready to receive data from a slave device, and low at all other times.
RDOUT	READ OUT. This signal is high when the master has placed valid data on the data bus for transmission to a slave device, and low at all other times.
RSACK	ACCESS. This signal is low during direct memory access cycles, and high during processor cycles.
RREF	REFRESH. This signal is low during memory refresh cycles, and high during other processor transactions.

Multibus

MWTC	MEMORY WRITE CYCLE. This signal is high when the master is writing to memory, and low during all other cycles.
MRDC	MEMORY READ CYCLE. This signal is high when the master is reading from memory, and low during all oter cycles.
IOWC	I/O WRITE CYCLE. This signal is high when the master is writing to I/O, and low during all other cycles.
IORC	I/O READ CYCLE. This signal is high when the master is reading from I/O, and low during all other cycles.

Appendix G

INTERFACE MODULE
6800/6802

INTRODUCTION

The Model 64672A Processor Interface, with the General Purpose Preprocessor, provides a complete interface between a 6800 or 6802 target system and the Model 1630A/D Logic Analyzer. The interface module connects the signals from the 6800 or 6802 processor to the logic analyzer inputs generating all status and clock signals required for inverse assembly of the 6800/6802 instruction set. Status is generated on the interface module to identify an opcode fetch when it occurs. This signal is used by the inverse assembler to provide a decoded listing of the data bus.

Table G-1. Interface Module Specifications

Processor Compatibility:	Motorola 6800/02 and all microprocessors that comply with motorola 6800/6802 specifications.
Maximum Clock Speed:	2 MHz clock input to microprocessor.
Signal Line Loading:	1 LS TTL load and approx. 35 pF capacitance.
Power Consumption:	Up to 0.8 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.
Environmental Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300 m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

SYSTEM CONFIGURATION

Minimum hardware requirements for state analysis of an 6800/6802 target system are as follows:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 072 which includes:

(1). 64672A Interface Module for 6800 and 6802 microprocessors, including an 6800/6802 interface circuit card and cable assembly.

(2). 6800/6802 inverse assembler and Format Specification setups on Minicassette HP Part No. 64672-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

The Model 1630D enables storage of up to 8 additional channels of information.

HARDWARE INSTALLATION

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recomments that you use RG-58, 4-foot or less to minimize voltage drop.

To connect the interface cable to the target system, lift the 6800 or 6802 processor from its socket, plug the interface cable into the processor socket, and plug the processor into the socket on the interface cable.

CAUTION

Care must be taken to align pin 1 of the cable assembly with pin 1 of the processor socket on the target system board.

Pin 1 of the cable assembly is labeled on the socket board and by the angled corner of the plastic pin-guard (see figure G-1). The 6800 or 6802 processor is then installed into the socket on the interface cable, again taking care to properly align pin 1. The socket on the interface cable is a Zero Insertion Force (ZIF) socket and must be opened before installing the processor. To open the socket, turn the small screw located at the pin 1 end of the socket. Secure the processor in the socket by turning the small screw in the opposite direction.

If a lower profile assembly is desired, the interface cable can be used without the ZIF socket. See figure G-1 for an exploded view of the interface cable assembly. Separate the ZIF socket by inserting a flat-blade screwdriver under the PC board located directly below the ZIF socket and carefully prying up. Care must be taken to avoid bending the pins of the ZIF socket or the interface cable. The interface cable assembly is plugged into the target system, and the processor installed in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if a lower profile is required. If the pin guard is removed, it is recommended that the 40-pin socket be plugged onto the bottom of the interface cable to protect its pins.

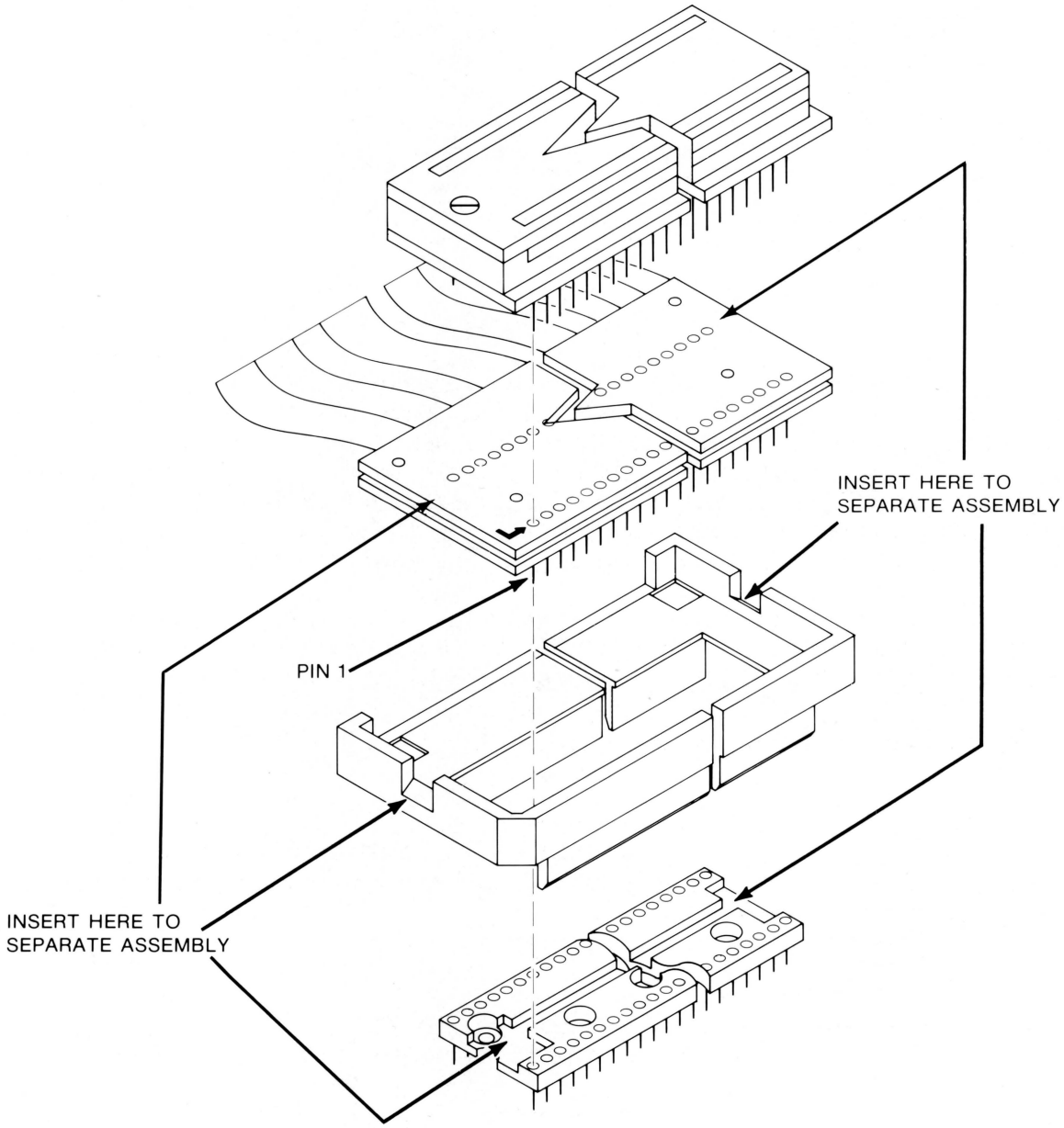

Figure G-1. Interface Cable Assembly, Exploded View

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	1
B	4
C	2
D	3
E	n/c

INTERFACE DESCRIPTION

The primary function of an interface module is to connect the target processor, through the preprocessor, to the analyzer in such a way that the address, data, and the status is available for the state analyzer to use. The 64672A brings the address and data lines straight through after buffering the signals. The 6800/6802 processor does not differentiate between a memory read and an opcode fetch. The 64672A makes this differentiation possible by means of a state machine on the interface module. The state machine takes the information on the data bus of the 6800/6802 target system and generates 4 bits of status for the analyzer.

The data bus from the processor is buffered before it is sent directly to the analyzer and to the state machine on the interface module (see the block diagram in figure G-2). The state machine consists of three PROMS that interperate the data to generate the status.

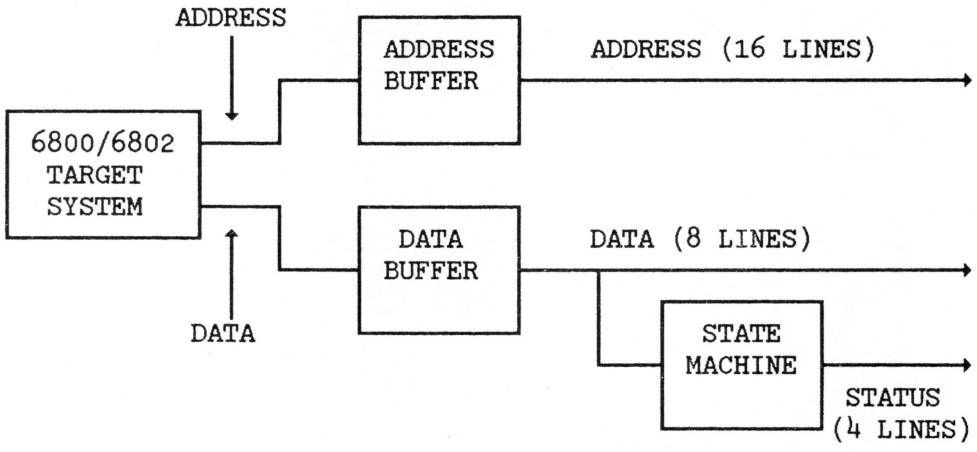

Figure G-2. Block Diagram of the 6800/6802 Interface

The inputs to the first PROM (U4E) are the 8 buffered data lines (D0 - D7) from the processor (see figure G-3). This PROM checks for any illegal opcode references and outputs one of 31 different codes. The code is based on the number of and type of cycles in the instruction. One of the codes is for an illegal opcode and another is to indicate that the state machine is out of synch with the processor. This 5-bit code is sent through a latch to the next PROM (U2E) where the number of cycles is determined and that information is sent through the latch to the inputs of U2E where the cycle count is decremented. The countdown continues for each instruction cycle, generating a 3-bit code for each cycle which is sent to the next PROM (U4F). This PROM takes that 3-bit code as input along with four status lines from the processor (VMA, R/$\overline{W}$, $\overline{HALT}$, DBE) and one signal generated on the interface board that determines when an interrupt vector is accessed. From all this information the final 4 bits of status is generated for the analyzer. These four status bits are used by the inverse assembler to decode the data lines. If, at any time in this chain of events, an illegal opcode is encountered the procedure is restarted until the state machine is synched to the processor.

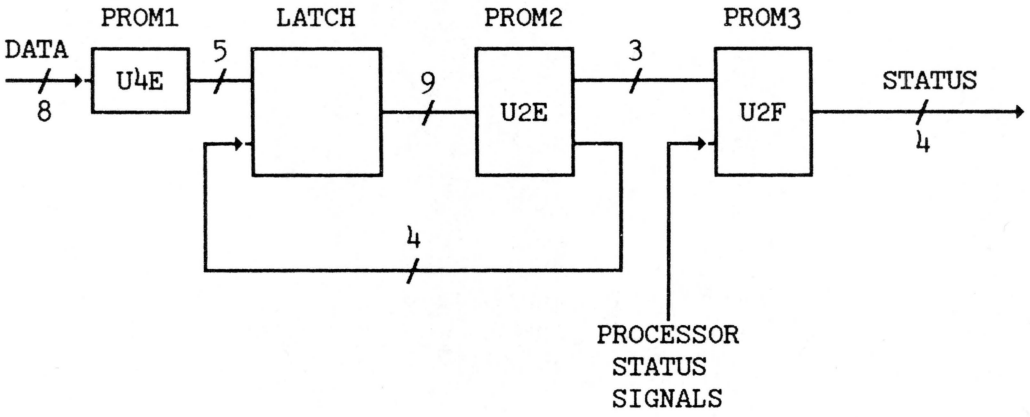

Figure G-3. Block Diagram of the State Machine For Decoding the 6800/6802 Status

Table G-2. 6800/6802 Signal List

CPU Signal	CPU Pin	Label	Pod	Bit
--	--	not used	0	0
--	--	not used	0	1
--	--	not used	0	2
--	--	not used	0	3
--	--	not used	0	4
--	--	not used	0	5
--	--	not used	0	6
--	--	not used	0	7
D0	33	DATA	1	0
D1	32	DATA	1	1
D2	31	DATA	1	2
D3	30	DATA	1	3
D4	29	DATA	1	4
D5	28	DATA	1	5
D6	27	DATA	1	6
D7	26	DATA	1	7
A0	9	ADDR	2	0
A1	10	ADDR	2	1
A2	11	ADDR	2	2
A3	12	ADDR	2	3
A4	13	ADDR	2	4
A5	14	ADDR	2	5
A6	15	ADDR	2	6
A7	16	ADDR	2	7
A8	17	ADDR	2	8
A9	18	ADDR	3	0
A10	19	ADDR	3	1
A11	20	ADDR	3	2
A12	21	ADDR	3	3
A13	22	ADDR	3	4
A14	23	ADDR	3	5
A15	24	ADDR	3	6
---	--	not used	3	7
---	--	not used	3	8

Table G-2. 6800/6802 Signal List (Cont'd)

CPU Signal	CPU Pin	Label	Pod	Bit
**	**	STAT	4	0
**	**	STAT	4	1
**	**	STAT	4	2
**	**	STAT	4	3
VMA	5	VMA	4	4
R/$\overline{W}$	34	R_W	4	5
$\overline{HALT}$	2	HALT	4	6
DBE *	36	DBE_RE	4	7
---	--	not used	4	8

* DBE for the 6800, always high for the 6802
** STATUS generated on the interface board

OPERATION

6800/6802 SELECTION

Because the two processors are so similar, the 64672A Interface is capable of connecting the state analyzer to either a 6800 or a 6802 processor. The differences between the two processors are the on-board clock and memory of the 6802. The interface module and cable avoid the possibility of loading the on-board clock of the 6802 by not connecting to those pins. Switch S1 must be set for the correct processor in order for the module to operate properly.

STATUS ENCODING

The total status field sent to the state analyzer by the interface module is 8 bits wide. These 8 bits are divided into 2 fields. The first consists of 4 status bits generated by the state machine on the interface module. The second field is actually 4 individual status signals from the processor. These signals are VMA, R/$\overline{W}$, $\overline{HALT}$, and DBE. For a complete description of the status field refer to the symbol map section in this chapter.

FORMAT SPECIFICATION

The configuration file (C6800:HP for both the 6800 and the 6802) contains a predefined Assignment menu for the format specification (see figure G-4). This assignment menu includes all the lables that are needed to monitor the 6800/6802 processors.

```
State Format Specification_____________________________________

[Assignment]                          Clock
                                       JKL
                  ------------------- [↓..] ------------------
Multiplexing    Pod4       Pod3       Pod2       Pod1      Pod0
   [ Off ]    [  TTL  ] [  TTL  ] [  TTL  ] [ TTL  ] [ TTL  ]
              8.......0 8.......0 8.......0 7......0 7......0
Activity>     _________ _________ _________ ________ ________
Label  Pol
ADDR   [+]  [......... ..******* ********* ........ ........]
DATA   [+]  [......... ......... ......... ******** ........]
STAT   [+]  [.....**** ......... ......... ........ ........]
```

Figure G-4. 6800/6802 Format Specification

The User Base menu of the format specification is set up with names to identify values found on the status label. See figure G-5.

```
State Format Specification_____________________

[User Base ]

_________________State Labels_____________________
Value      STAT
[BIN]
0000       illeg          (illegal opcode)
0001       oprand         (operand)
0010       exsub          (exit subroutine)
0011       ensub          (enter subroutine)
0100       sspul          (system stack pull)
0101       sspsh          (system stack push)
0110       halt           (halt)
0111       vectr          (interrupt or reset vector)
1000       dc             (don't care or unused)
1001       opcod          (opcode)
1010       dmard          (direct memory access, read)
1011       dmawr          (direct memory access, write)
1100       memwr          (memory write)
1101       memrd          (memory read)
1110       out_s          (state machine out of synch w/6800)
1111       intak          (interrupt acknowledge)
```

Figure G-5. 6800/6802 Status Map

TRACE SPECIFICATION

The 64672A Interface Card supplies status and a clock to the 1630A/D for every clock cycle. The trace specification can be configured to store only useful data and ignore the unused cycles of each instruction. Figure G-6 shows the trace specification for eliminating display of the unused cycles.

```
State Trace Specification_____________________________________

[ Single ] Trace Mode

In sequence
        [  Start  ] Trace at 00001 Occurrences of
        [any state] then store [≠a ]

Label› ADDR   DATA   STAT
Base › [HEX]  [HEX]  [HEX]

   a   XXXX    XX      8
   b   XXXX    XXX     X
   c   XXXX    XXX     X
   d   XXXX    XXX     X
```

Figure G-6. 6800/6802 Trace Specification

THE 6800/6802 INVERSE ASSEMBLER

The inverse assembler is designed to support both the 6800 and the 6802 with minimum user interaction with the system. The only operation the user must preform is to set the switch S1 on the interface module to the proper position. Since the instruction set is identical in the 6800 and the 6802, the same inverse assembler is used to decode both processors. If the switch S1 is set in the 6800 position when a 6802 is actually being analyzed, the inverse assembler will react to the RE signal. The RE signal enables and disables the on-board RAM of the 6802. When the on-board RAM is enabled (RE low), the inverse assembler will interpret all bus transactions as DMA transations. When the on-board RAM is disabled (RE high), the inverse assembler will decode the bus transactions correctly. To insure that all data is correctly interpreted and displayed for the 6802, switch S1 must be in the 6802 position. If switch S1 is in the 6802 position when a 6800 is being analyzed, the inverse assembler will not recognize any DMA transactions but all other bus transactions will be decoded correctly. In either case, there will be no electrical damage to the processor.

The 6800/6802 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that one byte of an expected (single or double byte) operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that both bytes of a double-byte operand were not stored.

Examples:

JMP	**57	indicates that high byte of destination address was not stored.
JMP	****	indicates that neither operand byte was stored.

In general, asterisks indicate that expected operand fetches are not stored in logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

Error Messages

The following list of messages will help you identify operation errors.

Data Error	-	trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.
illegal opcode	-	undefined opcode encountered. CPU action is indeterminate.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

Appendix H

Interface Module

NSC800

Introduction

The Model 64690A Processor Interface Module, when installed in the Model 10269A General Purpose Probe Interface, provides a complete interface between any NSC800 target system and the Model 1630A/D Logic Analyzer. The interface module connects all of the NSC800 target microprocessor signals to the logic analyzer inputs, along with all of the status and clock signals required for inverse assembly of the NSC800 instruction set.

The NSC800 configuration software on the mini-cassette sets up the [Assignment] menu of the logic analyzer format specification for compatibility with the NSC800 microprocessor. It also contains the inverse assembler routine required to obtain displays of NSC800 data in assembly language mnemonics. The interface module specifications are given in table H-1.

Table H-1. Interface Module Specifications

Processor Compatibility:	NSC800 and all microprocessors made by other manufacturers which comply with NSC800 specifications.
Maximum Clock Speed:	4 MHz.
Signal Line Loading:	One HCMOS load for all monitored signal lines plus approx 35 pF capacitance.
Power Consumption:	0.10 A at +5Vdc max, supplied by Model 1630A/D Logic Analyzer.
Environmental	
Temperature:	Operating, 0 to +55 degrees C (+32 to +131 degrees F); Nonoperating, -40 to +75 degrees C (-40 to +167 degrees F).
Altitude:	Operating, 4600 m (15 000 ft); Nonoperating, 15 300m (50 000 ft).
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

System Configuration

The minimum hardware required for analysis of a NSC800 target system consists of the following:

a. Model 1630A/D Logic Analyzer (with HP 82161A Digital Cassette Drive for inverse assembly).

b. 10269A General Purpose Probe Interface with Option 090 which includes:

   (1). 64690A Interface Module for NSC800 microprocessors, including an NSC800 interface circuit card and cable assembly.

   (2). NSC800 inverse assembler and Format Specification setups on Minicassette HP Part No. 64690-11000.

c. BNC cable assembly to connect +5V accessory power from logic analyzer to general purpose probe interface.

Hardware Installation

Install the interface module on the underside of the general purpose probe interface pod. Insert the free end of the interface card into the slots of the pod, then connect the pod internal cables to the interface circuit card, and fasten the cable end of the interface module to the pod using two screws.

Connect a BNC cable from the ACCESSORY POWER output on the rear panel of the logic analyzer to the ACCESSORY POWER input on the general purpose probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends that you use RG-58, 4-foot or less to minimize voltage drop.

Connect the interface cable to the target system by lifting the NSC800 CPU from its socket, plugging the interface cable into the CPU socket, and plugging the CPU into the interface cable. Be sure pin 1 of the CPU is installed in pin 1 of the cable socket. Pin 1 of the cable socket is identified on the CPU socket board and shown in figure H-1.

The CPU socket on the interface cable is a Zero Insertion Force (ZIF) socket. Before installing the CPU, open the socket by rotating the small screw located at the pin 1 end of the socket. To secure the CPU in the socket, rotate the screw in the opposite direction.

To obtain a lower profile assembly, the probe cable can be used without the ZIF socket. Figure H-1 is an exploded view of the socket assembly. Separate the ZIF socket assembly by inserting a flat blade screw driver under the pc board located directly below the ZIF socket and carefully prying up. Avoid bending the pins of the ZIF socket or probe cable assembly. Plug the probe assembly into the target system, and install the CPU in the cable socket. The plastic pin guard can be removed if it interferes with components of the target system, or if an even lower profile is required. Removal of the pin guard is not recommended, however, because this increases the danger of damage to the probe pins.

Connect the 1630A/D Logic Analyzer pods to the general purpose probe interface (Model 10269A) as follows:

Model 10269A Connector	Model 1630A/D Pod
A	1
B	4
C	2
D	3
E	n/c

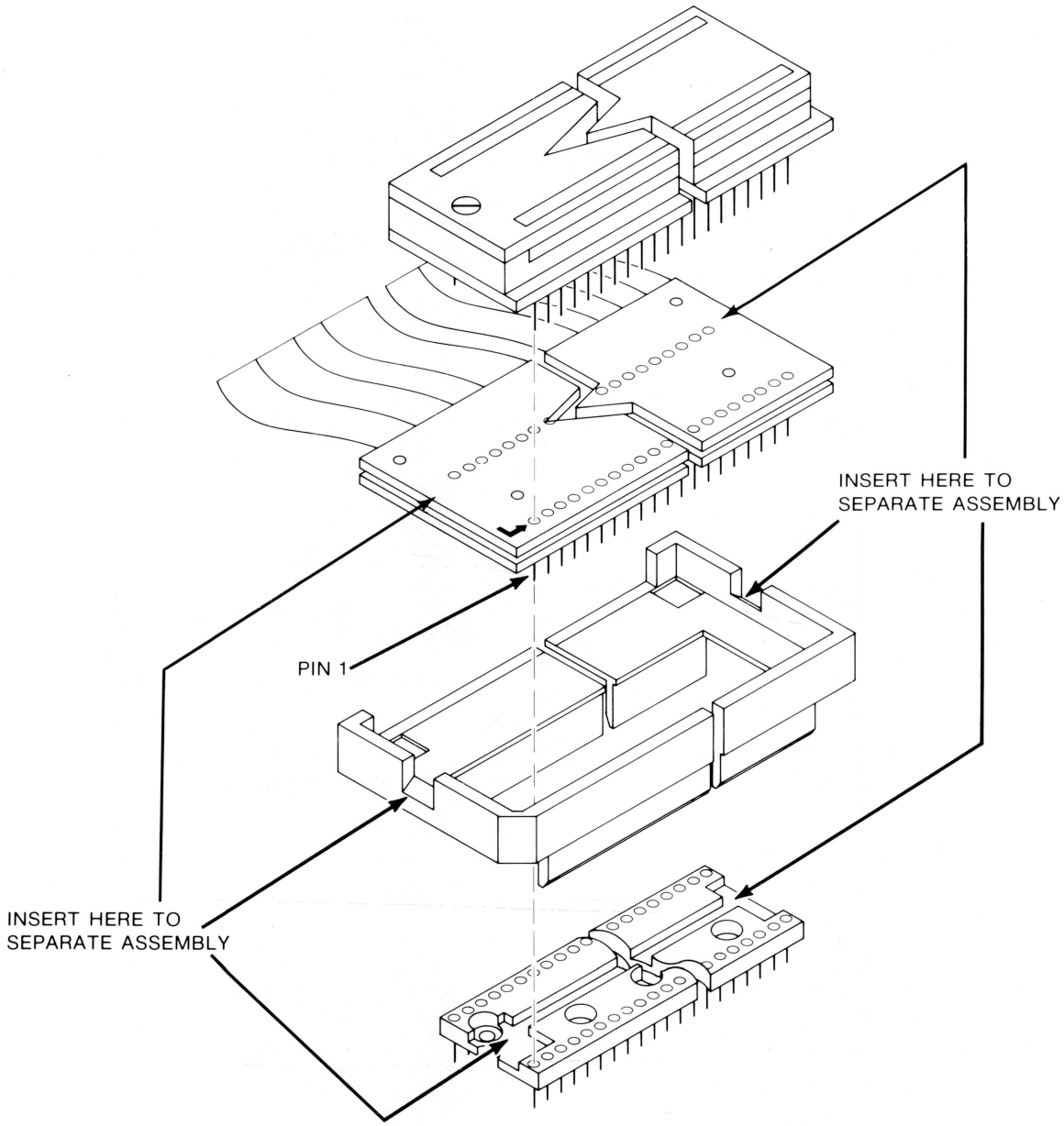

Figure H-1. ZIF Socket Assembly, Exploded View

Interface Description

The NSC800 interface circuit is comprised of buffers, latches, and gates. Generation and gating of some status signals to the general purpose probe interface is performed by the gates. Figure H-2 shows the NSC800 interface block diagram.

Table H-2 lists the CPU signals and cable lines on which those signals are carried to the logic analyzer.

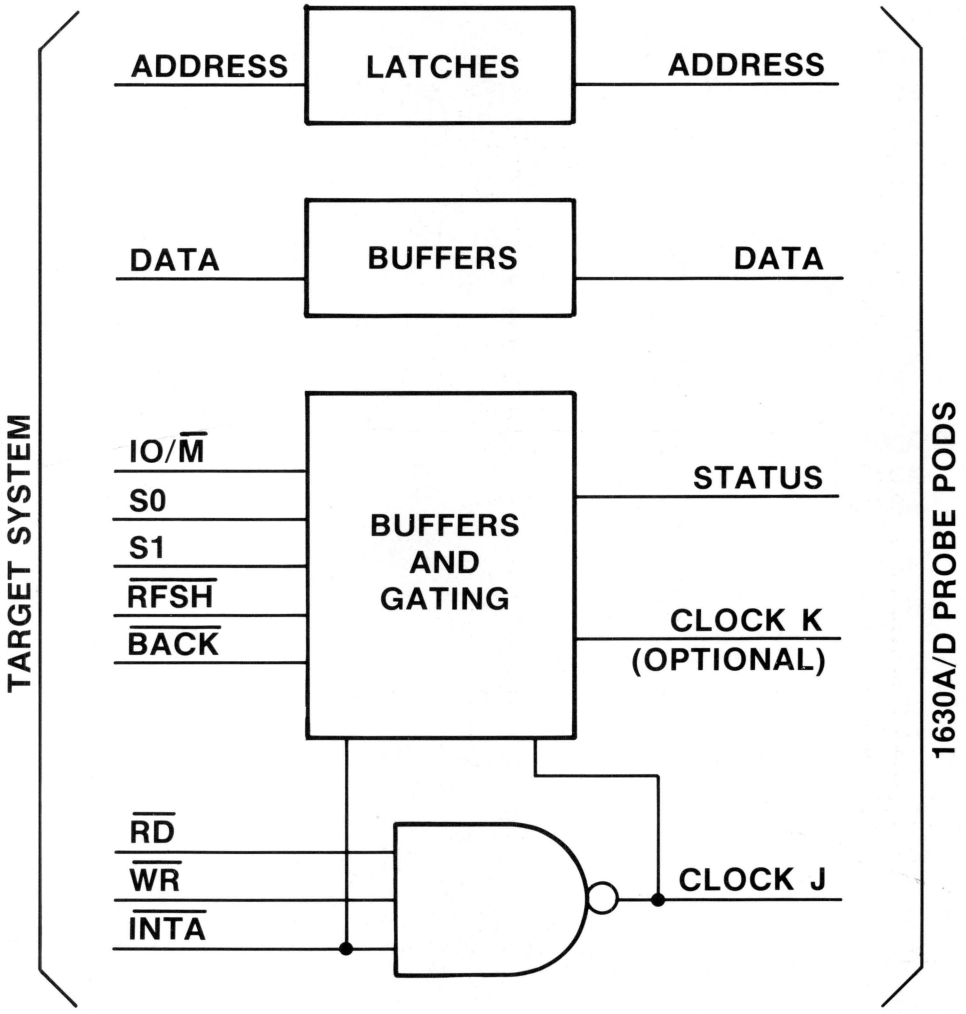

Figure H-2. NSC800 Interface Block Diagram

Table H-2. NSC800 Signal List

CPU SIGNAL	CPU PIN	LABEL	POD	BIT
---	--	not used	0	0
---	--	not used	0	1
---	--	not used	0	2
---	--	not used	0	3
---	--	not used	0	4
---	--	not used	0	5
---	--	not used	0	6
---	--	not used	0	7
AD0	12	DATA	1	0
AD1	13	DATA	1	1
AD2	14	DATA	1	2
AD3	15	DATA	1	3
AD4	16	DATA	1	4
AD5	17	DATA	1	5
AD6	18	DATA	1	6
AD7	19	DATA	1	7
AD0*	12	ADDR	2	0
AD1*	13	ADDR	2	1
AD2*	14	ADDR	2	2
AD3*	15	ADDR	2	3
AD4*	16	ADDR	2	4
AD5*	17	ADDR	2	5
AD6*	18	ADDR	2	6
AD7*	19	ADDR	2	7
A8*	1	ADDR	2	8
A9*	2	ADDR	3	0
A10*	3	ADDR	3	1
A11*	4	ADDR	3	2
A12*	5	ADDR	3	3
A13*	6	ADDR	3	4
A14*	7	ADDR	3	5
A15*	8	ADDR	3	6
---	--	not used	3	7
---	--	not used	3	8
IO/$\overline{M}$	34	STAT	4	0
S0	29	STAT	4	1
S1	27	STAT	4	2
$\overline{RFSH}$**	28	STAT	4	3
$\overline{INTA}$	26	STAT	4	4
$\overline{BACK}$	35	STAT	4	5
---	--	not used	4	6
---	--	not used	4	7
---	--	not used	4	8

* LATCHED
** GATED

Operation

The logic analyzer will automatically be configured for state analysis when you load the inverse assembler from the digital cassette drive.

Format Specification

When using the NSC800 interface module, the format specification will be set up by the mini-cassette software as shown in figure H-3.

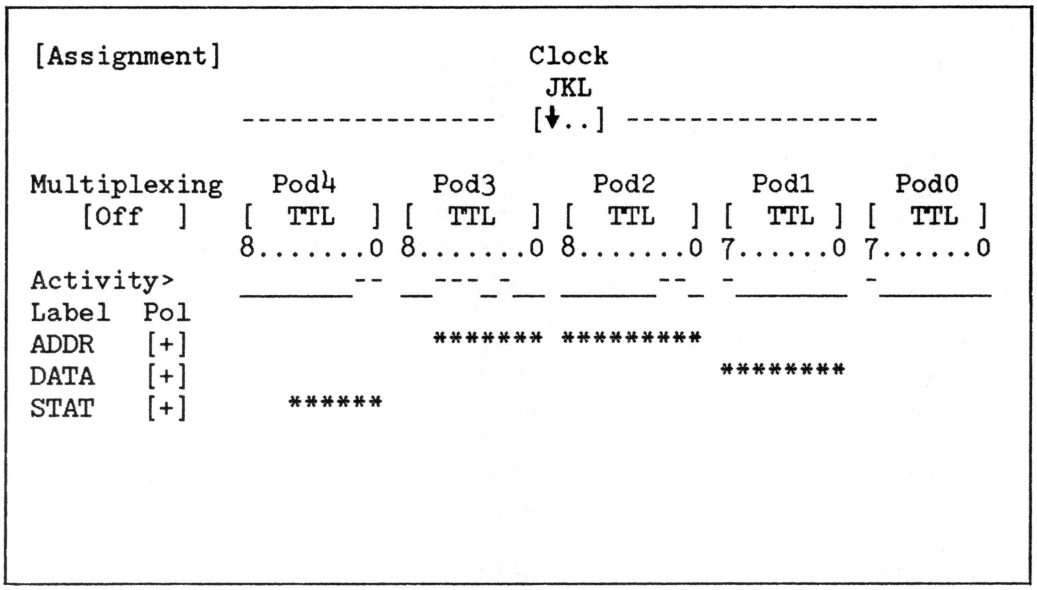

Figure H-3. NSC800 Format Specification

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for display in the trace list. Pertinent control and clock threshold levels are also part of the format specification.

The logical NAND of CPU signals $\overline{\text{INTA}}$, $\overline{\text{WR}}$, and $\overline{\text{RD}}$ is used as the clock signal to the logic analyzer.

The clock specification in Figure H-3 will capture all processor cycles except refresh. If refresh visibility is required, connect the $\overline{\text{RFSH}}$ line to Clock K, and add Clock K as a positive-edge transition in the OR'd clock field of the format specification.

The NSC800 Inverse Assembler

The NSC800 inverse assembler has been constructed so mnemonic output will resemble actual assembly source code. The few exceptions to this rule are detailed in the paragraphs below.

A pair of asterisks (**) displayed in the operand field of an instruction indicates that one byte of an expected (single or double byte) operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that both bytes of a double-byte operand were not stored.

Examples:

JP	**57	indicates that last byte of destination address was not stored.
LD	DE,****	indicates that neither operand byte was stored.

In general, asterisks indicate that expected operand fetches are not stored in logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

Error Messages

The following list of messages will help you identify operation errors.

Data Error - trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.

Illegal Opcode - undefined opcode encountered. CPU action is indeterminate.

Partial Instruction - an opcode (or opcodes) of a multi-opcode instruction was not stored in the logic analyzer.

NOTE

Make no modifications to the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Note also that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

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